AX32 LOW POWER EMBEDDED VIDEO ENABLED SYSTEM USING FPGA

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ABSTRACT

An architecture for embedded video and signal processing system is presented in this paper. The architecture is based on embedded microcomputer with ARM-based CPU and FPGA on the AX32 platform. While the CPU is necessary and integral part of the system, the signal and video processing tasks are "offloaded" to the FPGA in order to save computational power and energy. The target application is in standalone traffic monitoring systems with or without video processing and embedded sensory systems, e.g. in robots. Power consumption is critical as the applications are intended with battery power and also because in some applications, hermetic packaging not allowing cooling through e.g. flow of air must be used. The contribution presents a concept of the system, the video and signal processing approach, and draws some conclusions.

1. INTRODUCTION

Embedded systems play an important role in design of various devices for industry, traffic monitoring, home appliances and many more applications. The state of the art in computer science and technology allows for exploitation of signal and image/video processing; however, algorithms needed for these applications require a lot of computational power and tend to be also "hungry" from the point of view of electrical power consumption. This fact may cause troubles e.g. in battery powered applications or when heat dissipation is not desirable. Therefore, it is important to implement such algorithms in an efficient way and programmable hardware can play an important role in such implementation.

Scope of the article does not allow further in-depth analysis of previous work.

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2. SYSTEM DESCRIPTION

The proposed AX32 platform is highly modular. Base concept consists of two major devices - there is an ARM-based CPU and an industrial Xilinx Spartan-6 FPGA. This type of device will provide functionality and interface missing or inefficiently performed in the CPU. Communication between both of the devices in AX32 platform could be accomplished using shared serial port (e.g. SPI), shared parallel port (e.g external memory bus), or using dedicated digital I/O ports. The CPU also takes care about the 100Mbps Ethernet, the USB, or the SD/SHDC interface. CPU is also capable of other connectivity with another interface using its dedicated analog and some digital I/O ports.

Definition of physical interface is difficult in the context of changing single core ARM-based processor to another one (e.g. multicore). We used standard So-DiMM interface for interfacing processor with FPGA device and other peripherals. The reasonable So-DiMM modules so-called Colibri [1] are based on Marvell XScale PXA 320 [2] or NVidia Tegra T20 [3].

3. PROGRAMMABLE HARDWARE EXPLOITATION

The FPGA in AX32 system can be exploited for video preprocessing acceleration. It is possible to connect a video camera through the FPGA to the ARM-based CPU and place a pre-processing functional unit into the FPGA as shown in Figure 1. This unit (see Figure 2) can extend the image it acquires with an additional information obtained through preprocessing and still send such extended image to the ARM-based CPU through the dedicated Quick Capture Interface. The extended image is further described in [4].

Another suitable exploitation of FPGA in AX32 is radar signal processing (as described in [5] and [6]). The radar module is connected through an FPGA to the ARM-based

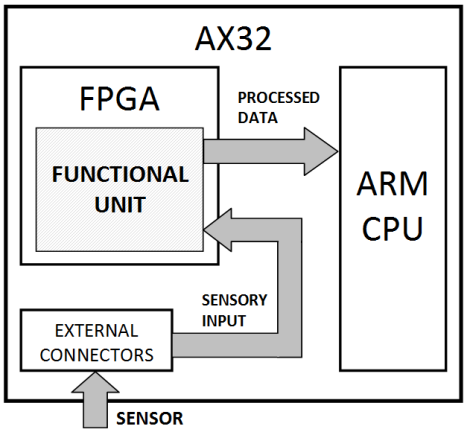

Fig. 1. The AX32 platform with functional unit in FPGA.

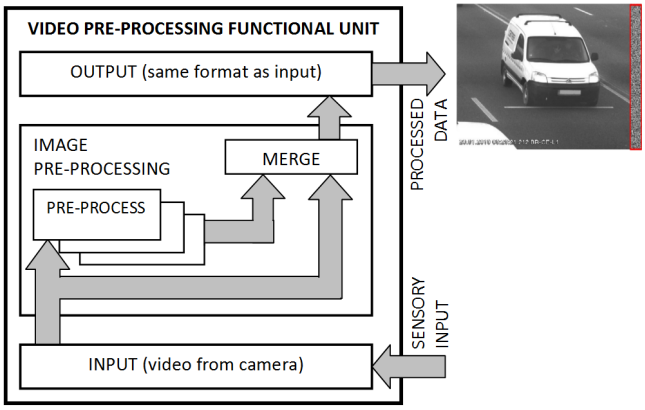

Fig. 2. The FPGA video pre-processing functional unit.

CPU similarly to the video camera in the previous example (see Figure 1). The functional unit in this case performs radar signal processing in order to determine velocity or distance of a detected object based on finding significant frequencies (see Figure 3). The frequency analysis performed by the bank of resonators is an interesting alternative to the typically used FFT (Fast Fourier Transform) especially for applications where fine frequency and time resolution is demanded. Computational complexity of resonators (implemented as an IIR system) can be easily compensated with using programmable hardware [7]. The FPGA resources (e.g. mutipliers, adders) have to be shared among more resonators whose inputs and outputs have to be multiplexed. Fortunately several optimization can be made [7]. The previously computed frequency spectrum can be send directly to the ARM-based CPU, or alternatively the more sophisticated post-processing in FPGA can be performed before.

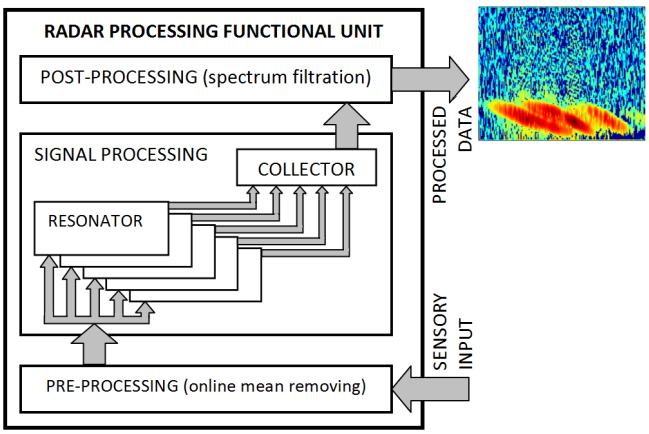

Fig. 3. The FPGA radar signal processing functional unit.

4. CONCLUSION

The contribution presented the new AX32 embedded video enabled embedded computational platform intended for low power high computational ability signal and video processing applications. The platform has been introduced along with samples of the intended video and signal processing applications. While the exploitation of the system is only at its beginning, it demonstrated nice capabilities and ability to be exploited in low power and battery powered application of signal and video processing.

Future work includes exploitation of the dual core NVidia Tegra and/or similar CPU, development of microprogrammed device and/or dedicated signal processing core in the FPGA and better integration of the FPGA with the CPU.

5. REFERENCES

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