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Setup for an Experimental Study of Radiation Effects in 65nm CMOS

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***Abstract*—Physical radiation experiments are a vital means for calibrating simulation models targeted to studying the impact of ionizing particles on VLSI circuits. However, their conduction requires special care and a very specific setup. In this paper we give an overview of such an experimental setup, and highlight some specific details. Beyond showing the context overarching the objectives of the experiments, the envisioned radiation sources, as well as design and architecture of a specific target ASIC, we will put specific emphasis on the communication infrastructure, namely an FPGA that controls the data exchange between some preprocessing infrastructure located on the target ASIC on one side and the host PC running the data analysis on the other. Finally, the physical arrangement comprising carrier PCB for the target ASIC, and cabling, which need to adhere specific requirements, will receive some attention as well.**

I. Introduction

It is well known that ionizing particles can cause malfunction of VLSI circuits [1]. Their effects, generally termed "Single-Event Effects (SEE)" can cause either permanent harm to the structures on the silicon (latch-up, burn-out, threshold shift), or cause bits to flip ("Single-Event Upsets (SEU)"). With the particle energies ASICs are normally exposed to, transient effects are far more frequent, and hence these are the main focus of the related research. Ionizing particles may originate in high energy cosmic radiation, partly indirectly via interaction with the atmosphere, or they may be caused by atmospheric neutrons hitting the silicon lattice. When crossing the junction of a transistor they deposit charge along their track, which is observed as a current pulse. This undesired current pulses, in turn, will cause voltage pulses across circuit impedances, resulting in so-called "Single-Event Transients (SETs)". The latter may be masked along their propagation path, by diverse mechanisms like RC filtering, logic gates, or closed latches [2], [3], [4]; but in some cases they will succeed in ultimately changing the value of a storage element, thus creating an SEU.

In spite of technological progress in making circuits more resistant against particle hits (like in layout, cell design etc.), this relative improvement is set off by trends like exponential scaling in the number of transistors per ASIC, exponential reduction in structure size (and hence critical charge), and (until recently) increasing clock frequencies. As a result, the SEU rates per ASIC not only increased significantly during the past (and are predicted to do so), their effects in the increasingly more complex circuits are also harder to understand and mitigate.

As a consequence, SET- and SEU-mitigation has evolved from a somewhat exclusive topic of fault-tolerant aerospace applications to an issue that is becoming relevant even for ground-bound commodity products [5]. Here, however, the cost pressure is much higher, and hence solutions that have been developed for the aerospace and critical-computing domain cannot directly be adopted. It is necessary to elaborate very cost-efficient solutions. Clearly, research in that domain requires suitable means for verification[1]. The most direct way of verifying a radiation tolerance mechanism is, of course, by physically exposing it to radiation. However, as usual with verification of fault-tolerance mechanisms, some means of fault-injection is required to artificially increase the fault rate – just putting the circuits into their intended environment would require way too long observation times before statistically meaningful amounts of fault data can be collected. In case of radiation tolerance this means exposing the circuit to a radiation source that produces a substantially increased particle flux, like the irradiation chamber of a nuclear reactor, a micro beam or the like. Unfortunately, access to these facilities is limited and complicated, and the preparation of such experiments costs a lot of money and efforts. This clearly makes simulation an attractive choice. In this domain, physical-level (TCAD) simulations present the most detailed view of the reactions caused by the particle inside the silicon. They allow to precisely choose all relevant properties of the particle like angle, energy, location, etc. However, for an accurate representation of the transistor structures, many details about the physical layout and the fabrication process need to be known (like doping profile, technology parameters, etc.) some of which are kept strictly confidential by the fab and hence not available. Furthermore, such simulations require a substantial amount of memory and performance and hence typically need to be confined to a couple of transistors only.

Another, very popular approach is analog simulation on circuit level (SPICE, Cadence Spectre) [6]. Here detailed simulation models for the circuit elements are readily available, and the model for the complete circuit compiled automatically by the synthesis tools. Also, due to the higher level of abstraction, circuits of reasonable size can be simulated with relatively limited performance. The remaining problem is how to represent the particle effect in the model [7]. Here the so-called double exponential current model according to equation (1) represents

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the state of the art [8]: It assumes a current source connected to drain or source of the affected transistor (with its other terminal connected to ground or positive supply, respectively), driving a current that exponentially rises, with a time constant of τ_R towards a maximum current of I_0, and then exponentially decays (time constant τ_F) back to zero.

$$I_P = I_0(e^{\frac{-t}{\tau_F}} - e^{\frac{-t}{\tau_R}}) \quad (1)$$

So far, this model is considered to reflect the pulse shapes actually seen in physical-level simulations and measurements most faithfully, and the intensity of the particle effect can be modulated by varying I_0 while the time constants are viewed as technology properties. However, it has been shown that upon closer inspection this model produces artifacts (overshoot, e.g.) and may have significant mismatch with pulse shapes seen in reality as well [9], [10]. An alternative model presented in [11] employs two current sources and seems to perform better, but still there is much room for improvement in this important topic. That is why in our projects EASET (Accelerator-based Experimental Analysis and Simulation Modeling of Single-Event Transients in VLSI Circuits; supported by the Austrian Science Fund (FWF) under project number P26435) and RoNaLD (Robust Nanoelectronic Logic Devices; supported by TU Wien) we are committed to elaborate an improved analog-level model for SETs that have a closer match with reality. The methodological approach of the project is to use physical radiation experiments for calibrating a TCAD model, which, in turn, will then be used for calibrating diverse instances of an improved SPICE model. In this way we hope to retain the ground truth observed during the physical experiments, while reducing the need for performing such experiments to a minimum. Clearly, to yield useful calibration data, such experiments must be carefully planned, starting from the selection of appropriate target circuits that shall be exposed to radiation, over efficient data collection and analysis, to the consideration of physical boundary conditions given by the radiation facilities. It is the purpose of this paper to summarize our efforts in creating such an experimental setup, with a focus on the two latter issues.

The paper is organized as follows: After the above introductory part that somewhat clarified the importance of radiation effects and the related studies, the next section will provide an overview of our experiment design. Subsequently, we will present the constituents of our setup, starting with the target ASIC in Section III, and continuing with the Controller FPGA (Section IV) and the software executed on the host PC (Section V). Finally we will give some insights on aspects of the carrier PCB for the ASIC as well as the bonding in Section VI, before concluding the paper with Section VII.

II. Overall Experiment Setup

A. Radiation Sources

The most relevant method for studying radiation effects in an ASIC would be to put this ASIC into its actual operation environment and observe the faults that occur over time. However, (fortunately) this "natural" rate of faults is normally too low to allow collecting statistically relevant data within a reasonable measurement interval. So, as usual with fault injection studies, the fault rate needs to be artificially increased. In our specific case this means exposing our ASIC to a radiation source that generates a higher particle flux (in the desired energy range). Here we basically have two options:

- In a **microbeam facility** the impact of particles can be confined to a very narrow area (below 1 micrometer in square) by means of a magnetic lense – within this area the local distribution is governed by statistics. Furthermore, the particle stream can be turned on and off very fast by an electrostatic switch, and while the beam is activated, the actual time of a particle impact is again governed by statistics. Here, however, average particle rate, particle type as well as energy are well known. Also, the actual impact of a particle can be detected (apart from the error it may create in the ASIC), by means of a channeltron, e.g., so even in case a particle does not create an error, its presence can be identified. If desired, the beam can be switched off after one particle impact and steered to the next position, yielding a single impact per location.
  With this type of source it is possible to clearly correlate the location of particle impact with the observed reaction, if the beam position control signals are recorded properly and some position reference is foreseen on the die. The whole die area may be systematically scanned, and specific regions may even be spared.
  The drawback of this approach is that in such experiments the particle type is typically fixed (exceptions are possible), and the particle energy is within a quite limited band. This is not very representative for the actual field operation.
  Physically, the fixture for the radiation target has a limited size (some 10cm), which has to be considered in the design of the carrier PCB for the target ASIC. It is, however, possible, to attach cabling to further components that are located outside the radiation area.
- In a **radiation chamber** we have "ambient radiation" created by a less controllable source like our atomic reactor at TU Wien. Here typically a larger spectrum of energies can be found (albeit on a generally lower level, since only neutrons are available), but there is no control over location of impact, and switching on and off the source is (in case a shutter is available at all) more difficult and less precise.
  The physical arrangement very much depends on the actual source. In our case, we have chosen to use the dry radiation chamber which allows more space for locating the target and its PCB, but at the same time the radiation is not so strictly confined to the chamber, so (rare) upsets in the components located outside the chamber need to be taken into account.

For the purpose of our investigations we want to use both types of facility, as both can deliver different views: In the micro beam we can precisely direct the particle beam to specific structures on our target (like a single inverter) and hence study the effect of particles on such structures in detail and in a very deterministic way (cause/effect). The radiation chamber in the reactor, on the other hand, is better suited for studying radiation effects in a statistical manner (relative sensitivity, e.g.), and it seems to resemble the actual

operation scenario more closely (although still type and energy distribution of the particles is different).

B. Target Arrangement

In order to collect the data of interest, we need to expose the target ASIC to the radiation and observe its behavior there, such as rate of upsets or propagation of SETs. For this purpose the bare die (a case would degrade the particle energy and make it more difficult to adjust the microbeam) is mounted to a PCB that is introduced into the radiation and allows some positioning options (angle, e.g.). Via cables the ASIC's input and output pins as well as its power supply are connected. Details about this can be found in Section VI.

The whole experiment is controlled by a PC that steers the ASIC's inputs and collects the readout data. In order to allow this PC to be located in some distance (several meters) to the ASIC, while at the same time avoiding long cables to unduly load the ASIC outputs, we decided to place an FPGA in between. This FPGA performs some preprocessing and, most importantly, a conversion from our very specific, optimized data transmission protocol to a standard protocol for which an interface is readily available on the PC (in our case RS232). So we have a control flow from PC to FPGA and then to the target, and a flow of readout data in the opposite direction. The overall architecture of our experiment setup is illustrated in figure 1. More detailed descriptions of its individual components will be given in the subsequent sections.

III. Target ASIC Architecture

The target ASIC comprises three different function blocks [12], [13], [3], [14]:

- The actual target circuits whose behavior under radiation shall be studied
- On-chip infrastructure to collect data from the targets
- A communication interface to the FPGA

We will present these components, one by one, in the following subsections; for more details see [12].

A. Target Circuits

It is known that the effect of a particle hit very much depends on layout and impedances of the circuit structures in the vicinity of the impact location. Therefore the choice of representative target circuits is important. Our choice here was to select one group of very common basic primitives like inverters or NAND gates, which gives very fundamental insights and allows comparison with existing literature.

As a second group we decided for basic sequential elements like the D-flip flop and the Muller C-element, which are the fundamental building blocks of synchronous and asynchronous designs, respectively.

Finally, as a third type of targets we use more complex circuits, like a Sklansky Adder.

To obtain a reasonable rate of particle hits even in the reactor, we placed multiple instances of each of these basic structures on our ASIC, thus effectively increasing the sensitive area. Furthermore we built chains and trees of basic elements. This again increases the chances of seeing particle hits and at the same time allows studying SET propagation.

B. Data Collection Infrastructure

The key purpose of this block is to collect the number of SETs seen in selected locations of the targets. To this end we have connected counters to those locations and count the transitions observed there during the measurement interval. Of course, the transitions caused by SETs are superposed with the regular activity of the target circuits. We have three solutions for this [3], which we apply depending on the actual target:

1) Operate the target in static mode: In the absence of regular activity each observed transition must be due to an SET. The downside is that we cannot obtain information of the SET behavior of the target under activity.
2) Subtract the regular transitions: Since the target activity is under our full control, we know exactly the number of transitions each target makes during the observation interval. So we can subtract that number from the recorded count. The problem here is that the counter needs to be wide enough to accommodate the sum of transitions, and in a typical observation interval of tens of seconds, the number of regular target transitions can be substantial.
3) Use difference counters: We can concurrently operate two or more targets and record only the difference of their transitions, assuming that an SET will only affect one target per observation interval. More specifically, we have elaborated a chain architecture of up/down-counters, each connected to different targets of the same type, which allows us to safely recognize even hits in multiple targets.

The problem we have with the data collection infrastructure in general is that it is much larger in area than the actual targets. While this is not a problem with the microbeam source, this means in the reactor experiments that we will see more SETs in the infrastructure than in the targets. We apply a twofold strategy to deal with this: In the first place, we obviously need to make our data collection infrastructure (specifically the counters) radiation tolerant, otherwise we cannot trust the collected results. This implies using larger physical structures (hardening by sizing) or some form of redundancy, both of which further increases the area and hence leaves less space on the die for target structures [15], [13]. So beyond devising an efficient architectural redundancy concept, our second strategy is to allow using the data collection infrastructure, specifically the counters, as targets as well. After all, they are comprised of the very same elements that we use as targets, namely D-flip flops and Muller C-elements, and if we can safely recognize SETs in them anyway, we can beneficially use the SET rates thus obtained in our statistics. We have also made a statistical analysis to make sure there is a reasonable chance to observe cases of particle hits in the actual targets, where the fault tolerance of the data collection infrastructure is not yet exhausted (by too many hits in itself) and the readouts can hence be used in statistics.

C. Interface

Finally, we need to transmit the counter states to the outside. Since we have quite a number of counters on our

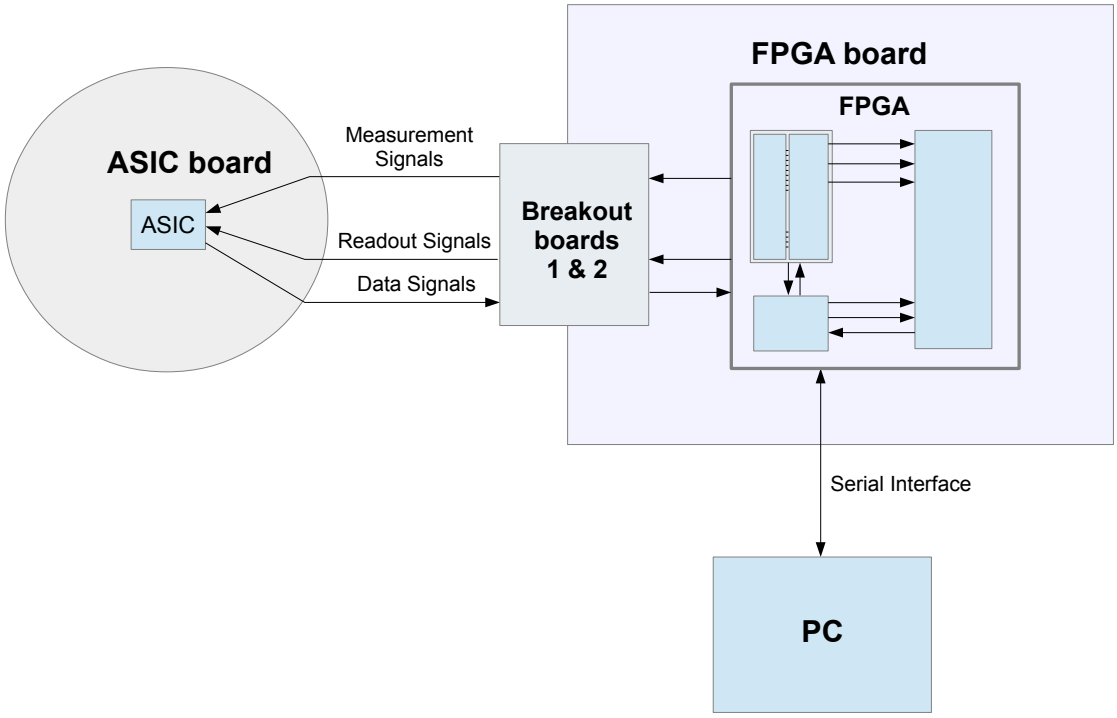

Fig. 1: Overview of the experiment setup

ASIC, we need to serialize data for transmission by means of parallel in / serial out (PISO) registers. We chose to use a reasonable number of such PISOs in parallel (each connected to an own output pin) to obtain a good compromise between required number of pins and transmission time. Table I gives an overview of the PISOs we have on our ASIC. The up/down-counters are denoted as "UDC", and the regular counters as "LFSR" as we have implemented those as linear-feedback shift registers.

TABLE I: Overview of PISOs

Target Circuit	Data Collection	PISO
inverter chain	2 32-bit LFSRs + 2 UDCs	84 bit
NAND-NOR tree	2 32-bit LFSRs + 2 UDCs	84 bit
flip flop chain	2 32-bit LFSRs + 2 UDCs	84 bit
elastic pipeline (Muller C chain)	2 32-bit LFSRs + 2 UDCs	84 bit
inverter chain	3 UDCs	30 bit
NAND-NOR tree	3 UDCs	30 bit
flip flop chain	3 UDCs	30 bit
elastic pipeline (Muller C chain)	3 UDCs	30 bit
Sklansky Adder	22 5-bit LFSRs	110 bit
inverter tree	15 5-bit LFSRs	75 bit
4:1 MUX	2 32-bit LFSRs + 2 UDCs	84 bit
4:1 MUX	3 UDCs	30 bit

Here again we have the problem of large area relative to the target structures, and again we decided to go for redundancy. However, to avoid spending area for hardware redundancy, we chose time redundancy here: Upon readout we capture and transmit the counter states three times each. This allows us to perform voting over these redundant readouts in the host PC. In some sense we use the counters as redundant units, from which we take three copies of the data. Note that the counters are protected by the means outlined in Section III-B, and errors in the PISO during other times than readout are not relevant.

D. Overall Layout

In order to allow for efficient experiments in the microbeam, we have arranged the layout of our ASIC in a ring-shaped fashion as shown in figure 2 in principle and in figure 3 in the layout; for more details see [14]

The idea is to facilitate concentrating the focus to the target circuits located right in the center, while not having any exposure of data collection infrastructure (unless desired when using it as target as well) and communication interface. To account for uncertainties in adjusting the focus we have introduced margins between the rings.

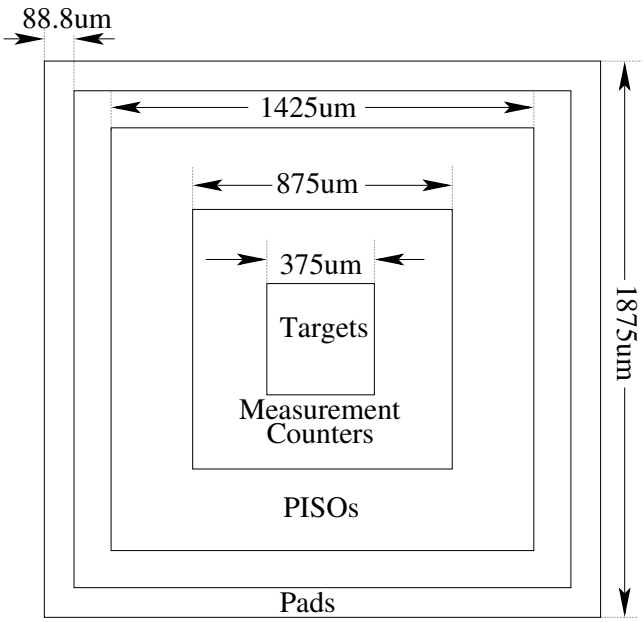

Fig. 2: Floorplan of the target ASIC

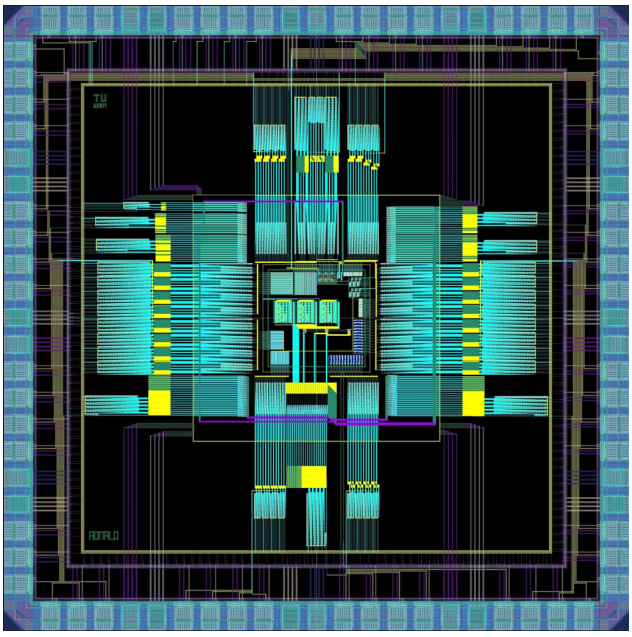

Fig. 3: Layout of the target ASIC

Figure 4 shows a photograph of the die.

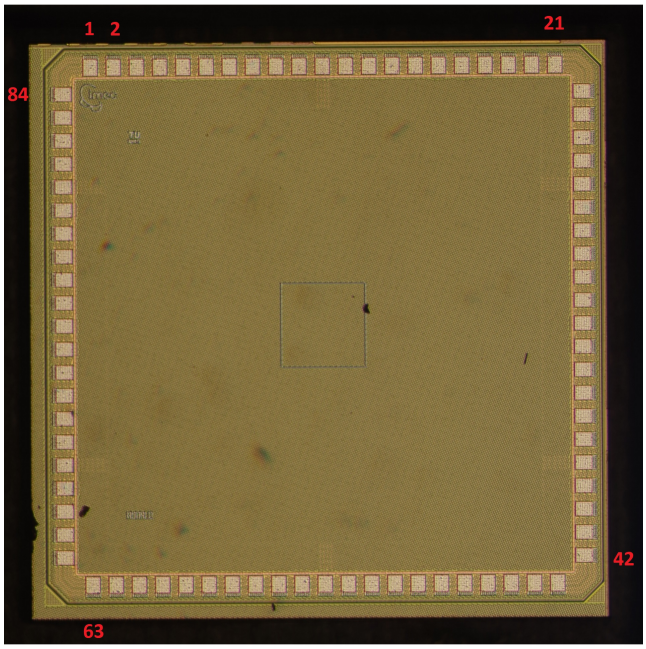

Fig. 4: Photograph of the die

IV. Controller FPGA

Figure 5 shows an overview of the Controller FPGA architecture.

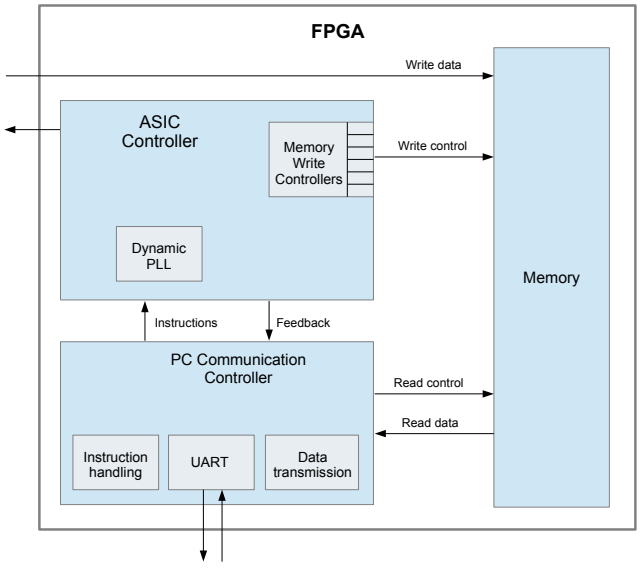

Fig. 5: Architecture of the Controller FPGA

The Communication Controller repeatedly sends “beacons” to the PC via the serial interface to show its presence. As the PC becomes available, it will respond with an instruction

message, containing the information about the measurement to perform. The message includes a hash which will be checked for correctness within the PC Communication Controller. If it is correct, the instruction is passed to the ASIC controller which in turn will start to process it. Once the ASIC controller gets an instruction it will start to configure the frequency of the measurement PLL according to the divisor and multiplier factors given by the instruction. This takes a few microseconds, after which the FPGA is ready to be triggered. It will signal its ready state to the surroundings on a 5V output pin, which can be used to trigger other external experiment equipment if needed. Once the measurement is triggered, it will initialize the ASIC by setting the counter values to their defaults and start the measurement.

After completion of the measurement, the ASIC controller will initialize the PISO readout and subsequently start the actual readout. It therefore activates the Memory Write Controller modules. There are six such modules, one for each kind of PISO. They generate the address and enable signals for the memory write accesses. Those memory control signals are synchronized with the data coming from the ASIC in such a way that the data transmission is possible with high frequencies, if crosstalk effects are avoided in the cabling. Also the cable delay is compensated by the framework. The memory elements used for storing the data have been implemented as a dual port RAM, so the read clock is independent of the write clock. Writing and reading are mutual exclusive in our design. This is beneficial for us, since it separates the two clock domains of the fast data signals coming from the ASIC and the slow read out accesses. The data of every PISO is stored in an own memory block and all data is stored in three different memory blocks as redundancy. So it can be ensured no data is lost if a memory cell breaks or if transmission between FPGA and PC temporarily fails. According to our time redundancy strategy all data will be read from the ASIC three times before the PC communication controller module is activated again in order to forward the data to the PC. The communication controller will now exclusively control the memory module. It will concurrently read out the data of one PISO type after another, pack it into 8 bit messages and transmit them to the PC. Once all ASIC data is transmitted to the PC, the FPGA sends its own status information such as the number of actual target clock cycles sent, failure codes, and whether it is ready for the next measurement. Then the procedure is over and the FPGA again starts to send beacons to the PC, indicating it is ready. The implementation has been kept as flexible as possible using VHDL constants. The PISO frequency, PISO scale factor, measurement scale factor, beacon interval and certain hold times can be adjusted, to mention just the most important settings.

V. Host Software

The software executed on the host PC can be divided into two major functions:

The **front-end software** is the part of the framework the user can directly interact with. Its main purpose is to send the measurement instructions to the FPGA, reliably communicate with the FPGA, monitor and log the FPGA controller status and store the measurement data. It can also be easily used by an external script which processes the measurement results and calculates the next measurement settings. This way radiation experiments can be fully automated and do not require human interaction.

The **analysis software** checks the data of the PISOs and gives the experiment operator immediate feedback about the results. In combination with the front-end software it can be used for establishing a control loop to keep a defined average of hits per experiment. Constants have been defined in the code to allow for quick changes in the settings such as the baud rate. It also offers direct access to its basic functions such as the calculation of the LFSR state after a certain number of transitions and the inverse function, finding the sequence number of a given LFSR state. The program parses the bit stream data file stored by the front-end software and groups the data by PISO. First it runs a redundancy check to see whether there have been transmission or storage errors. These kind of errors could be caused by radiation affecting the FPGA. Then it splits up the PISO data at the counter level. The expected counter values are known, hence deviations caused by SETs can be identified. The diagnosis can be based on fault dictionaries that associate with every readout the most probable SET scenario that may have caused it. The elaboration of such fault dictionaries is very challenging, but the software can then just make direct use of them.

VI. Physical Arrangement

For the cabling between the FPGA and ASIC boards using FMC compatible cables[2], breakout boards in combination with ribbon cables and breakout boards in combination with coaxial cables have been considered. Coaxial cables would make the handling of the cables difficult, as there are many signals. FMC cables are expensive and difficult to mount on the PCB. So it has been decided to use breakout boards with ribbon cables for the validation setup. They may not be optimal for high frequency signals, but offer a high number of pins and are the most simple to handle. For high frequency setups it is easily possible to exchange the cables using another ASIC PCB.

In order to allow an easy access to the various features built inside the ASIC chip and most importantly to facilitate the observation of its behavior during the radiation-focused tests, a dedicated carrier board has been developed. In fact, it involves double-sided printed circuit board (PCB) based on FR-4 substrate. Due to the specific nature of radiation chamber setup and the focused-beam with ionizing particles all the conductive tracks on this PCB had to be made with 18um copper foil laminated on from both sides of the FR-4 substrate of 1.5mm thickness. The intention is to mount the ASIC on top of the PCB using the wire bonding attachment technique. In addition, this carrier board is equipped with number of connectors and other auxiliary electronics features that are necessary for establishing a reliable link with the main processing card based on FPGA technology. It also contains a set of alignment holes for the radiation chamber enclosure.

Standard surface coating of the PCB, which is suitable for soldering of electronic components, may include e.g. chemical thin, hot air solder leveling or similar process. However, these methods typically do not provide steady foundation for wire bonding connections. A special surface treatment is therefore

[2]FMC is an ANSI standard and stands for “FPGA Mezzanine Card”

necessary for the creation of reliable links between the mounting pads available on the ASIC chip and the underlying PCB on the other side. In this case the attachment locations on the PCB, which are made of thin copper foil, were further covered with electroless nickel and immersion gold layers (ENIG). From a technical point of view, ENIG typically consists of two-layer metallic coating of 2-8 μm Au over 120-240 μm Ni. The purpose of Nickel is to establish the barrier to the protrusion of copper particles, which could lead to the unwanted oxidation effect and further impact the reliability of wire bonding. In addition, the gold protects the nickel during storage and also provides the low contact resistance required for the thin gold deposits.

The process of connecting the ASIC chip to the carrier PCB basically involves two steps. First of all, the carrier board contains a dedicated area of 3mm x 3mm dimensions within its center part for assembly of the ASIC. Due to the fact that the backside of the chip does not require conductive connection to grounding or power supply rails, a one-component epoxy based glue Epotek H31D with Ag filler was used for its permanent attachment. The second stage takes care of the signal path which is electrically linking together the active structures of the ASIC with the rest of PCB. Individual layers that make up the mounting pads on the chip surface have material and geometrical arrangement facilitating the interconnection using micro-wire. Of course, the carrier PCB has to come up with suitable surface coating as well, which is ensured in this case with the ENIG process. Layout of the mounting pads on the PCB was is organized into specific pattern around the mounting area for the ASIC in such way that the length of wire bonding connections is minimized and their mutual contact avoided.

The material of the contacting wire typically involves an alloy of copper, aluminium, gold or similar. In this particular case the gold bonding micro-wire of 25μm diameter was used. A semi-automated wire bonding station HB16 played a key role in the successful deployment of this process. It is important to point out that the wedge method (see figure 6) with thermosonic principle of join formation was used. This method of wire bonding involves the heat delivered through the working table and also ultrasonic energy coming from the tip of contacting tool, which also applies a certain amount of pressure onto the contacting wire. The automated movement of its contacting arm offers substantial benefits for the proper loop shaping of the contacting wire. In fact, it is necessary to form a kind of loop that allows to go safely across the edge of the ASIC towards the mounting points on carrier board (see figure 7), to which the ASIC is glued, and also ensure the overall quality of such joint on both sides.

The wire bonding process typically requires a careful definition of numerous parameters. For example, pre-heating temperature of the working table of this bonding station was set to the range of 50 to 80°C, ultrasound frequency was set to 62kHz and its power to approximately 250mW to 270mW, time range between 220ms to 250ms for the actual joint creation and tip pressure force of 250nCm to about 300nCm. The working tip 4445-1520-3/4-CG-F-BKCER was used in this case as an important element within the specific setup of wire bonding process. The transverse groove on the tip helps to maintain an appropriate fixation of the bonding wire during the induced oscillations of the tip itself[3].

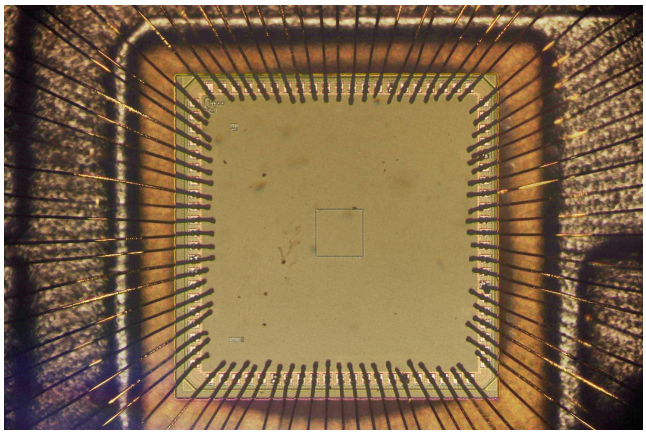

Fig. 6: Photograph of the bonded die

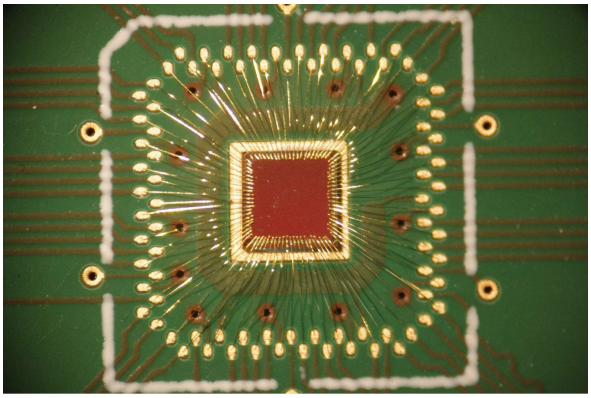

Fig. 7: Photograph of the ASIC mounted on the carrier PCB

VII. Conclusion and Future Work

In this paper we have presented an overview of our setup for physical radiation experiments, intended to study the impact of particle hits on 65nm CMOS and, based on that, elaborate an improved SET model for analog-level simulation. One peculiarity of our approach is to use both, a well targeted particle beam from microbeam facility as well as ambient radiation in the dry radiation chamber of a nuclear reactor as sources, in order to leverage the specific strengths of both approaches. This had immediate effects on the design and layout of the target ASIC: We have physically separated target blocks from infrastructure blocks (data collection, interface), and we had to make the latter radiation tolerant.

We have also reported on the Controller FPGA that we use to interface our target ASIC with the host PC and sketched its

[3]Page 110 in following material contains a detailed view of the tip and contacting wire: http://www.tpt-wirebonder.com/uploads/media/2016_Gaiser_Coorstek_-_Catalog_01.pdf

architecture. Furthermore we have presented the key features and structure of the software that is executed on the host PC to control the experiments and analyze the collected data.

Special consideration was also given to physical arrangement, like the requirements on and design of the carrier PCB for the target ASIC, as well as the associated bonding.

Currently the whole setup is ready to go, and we plan to perform the first experiments in a nuclear reactor within the next months – although the target ASIC is only partly functional and a re-design is ongoing in parallel. Microbeam experiments will follow, as soon as access to a microbeam facility is possible.

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