Multidimensional Pareto Frontiers Intersection: Processor Optimization Case Study

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Abstract

Almost all today's electronic devices are equipped with a processor. Different applications require and depend on different properties of the processor. For example, the fast-growing field of Internet of Things depends on a long operation time of the devices when powered with batteries. Using general purpose processors has proved ineffective which led to a growing usage of Application-Specific Instruction-Set processors (ASIPs) which can be optimized for specific applications using different modifications of their properties (such as the number of registers, cache sizes, instruction set modifications, etc.).

A suitable processor configuration can be hand-picked by a designer or by an automatic tool. Such a tool was developed in our previous research. It is able to find a set of Pareto-optimal processor configurations for a specific application which can be a significant help in a device design. The cost of the design process can be cut significantly when a processor is used in multiple designs. The goal of this paper is to introduce a tool able to find a suitable processor configuration for multiple applications by constructing a compromise Pareto-optimal frontier of processor configurations. The paper describes this problem on a theoretical level and it also introduces a practical implementation and experimental evaluation of constructing a compromise Pareto frontier of processor configurations for a set of applications. The experiments are based on a parametrizable RISC-V processor and example of compromise Pareto-optimal frontier is shown in Fig. 1.
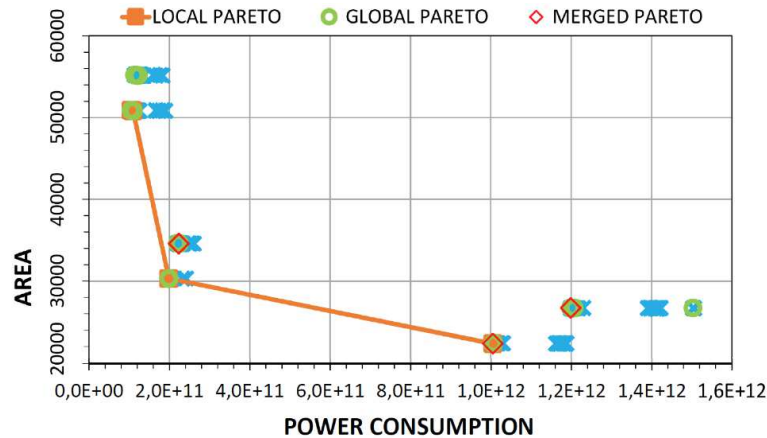
Fig. 1: An example of all configurations (blue marks) with the original local and global Pareto frontiers together with merged Pareto frontier.

Paper origin

The original paper has been accepted at 22nd Euromicro Conference on Digital System Design in Kallithea, Chalkidiki, Greece [1].

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References

[1] J. Podivinsky, O. Cekan, M. Krcma, R. Burget, T. Hruska and Z. Kotasek. Multidimensional Pareto Frontiers Intersection Determination and Processor Optimization Case Study. In: 2019 Euromicro Conference on Digital System Design. Kallithea: IEEE Computer Society, 2019, accepted for publishing.