Modelling and Physical Implementation of Ambipolar Components Based on Organic Materials

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***Abstract*—Systematic effort dedicated to the exploration of feasible ways how to permanently come up with even more space-efficient implementation of digital circuits based on conventional CMOS technology node may soon reach the ultimate point, which is mostly given by the constraints associated with physical scaling of fundamental electronic components. One of the possible ways how to mitigate this problem can be recognized in deployment of multifunctional circuit elements. In addition, the polymorphic electronics paradigm, with its considerable independence on a particular technology, opens a way how to fulfil this objective through the adoption of emerging semiconductor materials and advanced synthesis methods. In this paper, main attention is focused on various aspects standing behind the conception of polymorphic electronics together with a number of important benefits that can be obtained with the introduction of ambipolar elements. Besides that, relevant equivalent circuit models of the selected ambipolar components are presented in conjunction with the experimental results. However, key aspect depicting the novelty of the presented approach is primarily based on the hybrid combination of an initial chip infrastructure platform with the subsequent deposition of suitable organic semiconductor layer showing ambipolar property. Finally, the applicability for construction of real multifunctional circuits is assessed.**

Keywords—digital circuits; reconfiguration; multifunctional logic; ambipolarity; polymorphic electronics; organic materials

I. INTROCUTION

Seemingly endless trend of downscaling CMOS technology features in almost linear manner according to the Moore's law [1], as it was a rather common practice during several previous decades, has enabled the semiconductor industry to fit an ever-increasing number of devices per unit area and also achieve higher performance expressed as unit of energy (watt) spent in performing computational tasks. Various research directions have been mostly addressing possible ways how to achieve even a greater scaling of the technology features in order to push the actual integration level further beyond the existing boundaries. Nevertheless, the existence of physical limits to this growth is generally recognized today: the electronics-based technologies cannot be scaled down beyond certain dimensions that are inherently defined by some physical constraints [2].

Nowadays, it is possible to identify a diverse range of application areas where a digital circuit with the naturally built-in capability to perform a set of different functions at particular moments in time may prove to be a very efficient means of solution. Obviously, the most straightforward approach how to address this peculiar need is to design as many different circuit variants as the overall number of functions that are actually needed in a given situation, and switch them accordingly. The obvious drawback behind this conception, and its essential limitation as well, will emerge in a direct connection with the overall size of the resulting implementation on the circuit level that needs to be placed into a target chip estate of a restricted dimensions.

Recent advancements within the field of digital design techniques and components for digital circuits provide a vital evidence that yet another feasible strategy may be employed – area and time-efficient circuit design based on utilization of individual structural elements exhibiting multifunctional nature [3]. In this case, the entity of multifunctional circuit is devised as a compact structure involving set of multifunctional components, where their mutual, low-level interconnection scheme remains untouched in all permissible operating modes and only the active function of these components is expected to change intentionally.

A special case related to these multifunctional circuits is based on the adoption of polymorphic electronics approach [4]. Such circuits typically change their function in accordance to the actual state of a target operating environment, which is represented by a physical quantity with notable influence on some of the physical parameters of electronic structures – power supply voltage level, voltage amplitude of a signal, temperature, etc. In addition, no configuration network with a global scope or dedicated input pins of these components are required [5]. It's important to point out that change of the active function, which is executed by the polymorphic circuit, takes place immediately without no eminent delay.

Today's applications are generally based on exploitation of unipolar semiconductor transistors. However, the concept of polymorphic electronics has more profound nature and allows to conveniently employ new emerging devices with the ambipolar behaviour. In fact, relevant aspects of the emerging materials and technologies can be approached from various standpoints through the formulation of several abstraction levels [6]. Without the ambition to provide their complete and exhaustive list, the most interesting candidates for a potential replacement of unipolar CMOS technology in the suggested

scenario may include silicon nanowires (Si-NWs) [7, 8], carbon nanotubes [9, 10], graphene nanoribbons [11, 12], organic polymers with semiconductor-like properties [13], and presumably even other suitable emerging nanostructures and materials [14] which make it possible to obtain new generation of advanced multi-functional logic elements.

The structure of this paper is organized as follows: the opening section explains the basic aspects of multifunctional circuits. Section II is briefly explaining key notion behind polymorphic electronics and the benefits to be obtained when using ambipolar components. Then, ambipolar transistor model is shown in section III together with a specification of basic components. Behaviour analysis of the inverter structure based on the model is provide in this section as well. Physical fabrication of ambipolar devices based on hybrid integration of the chip platform and an organic layer is summarized in section IV. Finally, section V provides the conclusion of this paper.

II. Polymorphic Electronics

The notion of polymorphic electronics [4] determines, in its own essence, a standalone category of reconfigurable circuits, which represents a very attractive pathway how to implement all the required functional properties in a resource-efficient way. In case of circuits assuming the principles of polymorphic electronics, set of various modifications projected into the key physical characteristics of fundamental components (e.g. in a transistor's operation point, usage of ambipolar charge carrier conductivity) are predominantly involved behind the change of their behaviour as a direct response to the influence of external stimuli – temperature, power supply voltage, light intensity, special signal, etc. However, the structure of the circuit itself remains unchanged on the interconnection level for all the intended functions.

TABLE I. Overview of existing polymorphic gates.

Gate	*Value*	*Cntrl.*	*Size*	*Ref.*
NAND/NOR	3.3/1.8V	V_{dd}	6	[16]
AND/OR	1.2/3.3V	V_{dd}	8	[17]
NAND/NOR	5/3.3V	V_{dd}	8	[18]
AND/OR	27/125˚C	temp.	6	[4]
AND/OR	5/90˚C	temp.	8	[4]
NAND/NOR	0/5 V	ext. voltage	10	[20]
NAND/NOR	5/0 V	ext. voltage	8	[21]
NAND/NOR	5/0 V	ext. voltage	10	[21]
NAND/XOR	5/0 V	ext. voltage	9	[21]
AND/OR	0/3.3 V	ext. voltage	6	[4]
AND/OR/XOR	3.3/1.5/0 V	ext. voltage	9	[4]
NAND/NOR	0/5 V	ext. voltage	10	[19]

A. Survey of existing polymorphic gates

It is symptomatic that the availability of suitable building components can be identified as one of the key prerequisites enabling the practical deployment of polymorphic circuits. As it is demonstrated in Table I, there already exist a number of polymorphic gates which are implementing various functions. These gates were mostly constructed by means of using certain variation of conventional CMOS fabrication process. Main drawback in this case can be attributed precisely to the fact that it is necessary to use transistors with different channel width and length dimensions in order to achieve the desirable polymorphic behaviour. This observation also explains the reason why individual transistors in such circuitry may also operate in a linear mode instead of adhering to the switching mode only. As a consequence steady current flow through such gates leads to a significant rise in power consumption.

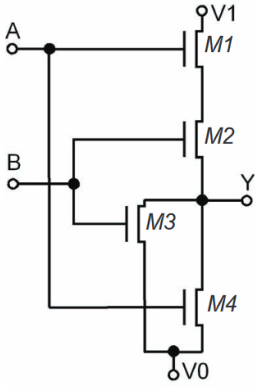

Fig. 1. Polymorphic NAND/NOR gate using ambipolar transistors.

B. Benefits of amnipolarity

Therefore, unconventional approach to the construction of polymorphic gates using technologies such as transistors with ambipolar characteristics [15] is highly desirable. These gates contain less transistors and, unlike previously adopted CMOS scheme involving various tweaks, also operate exclusively in switching mode. An example of ambipolar polymorphic gate is given on Fig. 1 above. This gate exhibits NOR function when transistors M1 and M2 are in N-mode and transistors M3 and M4 are in P-mode. When polarity of all the transistors is changed, NAND function is exhibited by the gate itself. The polarity of transistors, and by this the function of the gate, is controlled by power source – polarity of voltages V0 and V1.

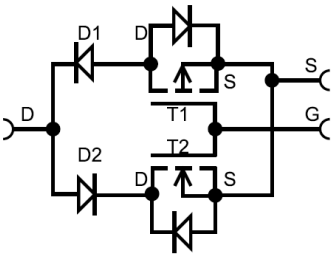

Fig. 2. Basic model of an ambipolar transistor.

III. Ambipolar Transistor Model and Components

This section is dealing with a definition of fundamental model for ambipolar transistors, which are important means how to describe the operation of polymorphic gates. Figure 2 above shows an example of ambipolar transistor model created by means of utilizing conventional silicon MOSFET transistors. For the construction of such a model, transistors with terminated substrate would be preferable. Unfortunately,

such transistors are rare, so the model was created from the standard P – type and N – type transistors. Each instance of the unipolar MOSFET transistor used there has an integrated body diode where its unwanted influence must be eliminated by anti – serial connection of diodes D1 and D2.

A. *Principles of ambipolar transistor model*

The function of this model is explained in details within Table II below. Its columns D, S, G denotes the individual terminals of the transistor model; their values are + or -, which corresponds to the supply voltage polarity (Vcc, GND). Then, columns D1, D2 simply denote anti-serial diodes from transistor model and have values of F (forward direction) or R (reverse direction). Columns T1 and T2 are related to transistors from the same model. If a value is ON, the transistor is closed (current flows through the transistor), while OFF signature denotes that transistor is open (and therefore current cannot flow across this element). The last column depicts the behaviour of the model where HiZ represents the high impedance state (model is "tri-stated"). "Close" option simply means that the model is closed and the conductive pat his available for current.

TABLE II. OPERATING STATES OF AN AMBIPOLAR TRANSISTOR MODEL.

D	*S*	*G*	*D1*	*D2*	*T1*	*T2*	*D-S*
+	-	-	R	F	OFF	OFF	HiZ
-	+	-	F	R	OFF	ON	Close
+	-	+	R	F	ON	OFF	Close
-	+	+	F	R	OFF	OFF	HiZ

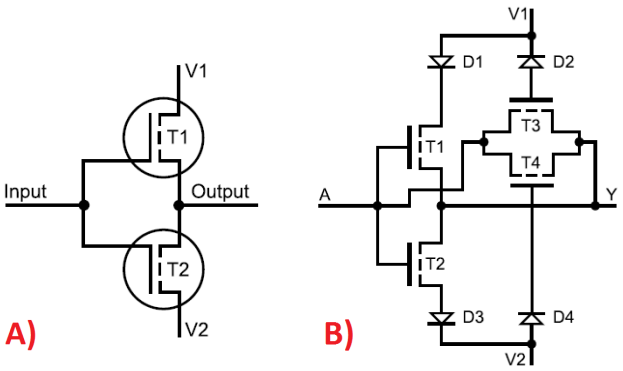

Fig. 3. Inverter structure (A) and polymorphic gate with the function of negation/idnetity (B) using the ambipolar transistor model.

B. *Ambipolar inverter and negation/identity gate*

The simplest gate made of the ambipolar transistors is an inverter. Unlike to the conventional CMOS-based one, when the ambipolar transistors are used, both are of the same type, see Fig. 3 above. It means that these transistors will autonomously select their operating mode with respect to the actual placement inside a given circuit. This makes the ambipolar inverter resistant to power supply polarity change – if the polarity assignment of V1 and V2 is swapped, the type of transistors will change. Finally, negation/identity gate is shown on Fig. 3 above as well.

IV. FABRICATION OF AMBIPOLAR ORGANIC TRANSISTORS

Set of physical OFET devices were fabricated according to a bottom gate, bottom contact geometry on heavily doped Si wafers obtained from Fraunhofer IPMS [22], with a 230 nm SiO2 layer with 30 nm Au electrodes on a 10 nm ITO adhesion layer. Two different architectures of substrates were used. First with 16 single transistors with different channel lengths (4x (2.5, 5, 10 and 20 um)) and a width of 10 mm. Second architecture was up to 36 single transistors are interconnected to inverters and ring. The electrodes at second architecture had different channel lengths (L = 2.5, 5, 10, 20 and 40 um) and a width of 2 mm. Organic semiconductors of Tips-Pentacene, PCBM-C60 and P3HT solution were deposited by spin coating a 15 mg/ml solution at 1500 rpm on both architecture. In order to handle the electrical measurement of the fabricated chip in an easy way, a dedicated chip expander platform (see Figure 4 below) was designed.

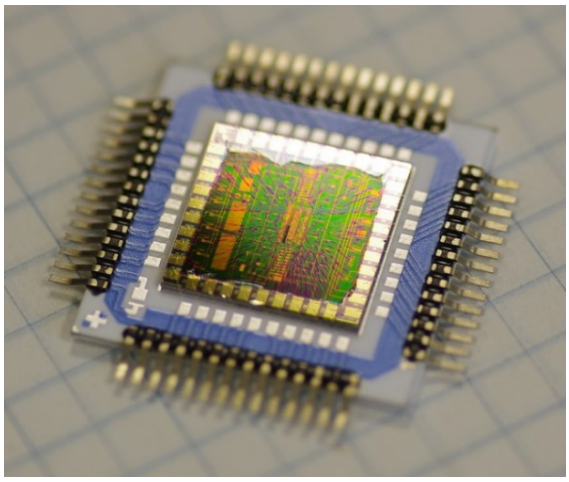

Fig. 4. Experimental hybrid semiconductor device mounted on the chip expander platform and interconnected by golden wires (wirebonding).

V. CONCLUSIONS

The recently achieved results indicate that the ambipolar property may turn out very supportive in connection with the attempt to improve the implementation efficiency of either various existing polymorphic circuit blocks or to develop completely new circuit structures, especially when compared to the previously used modifications of otherwise conventional techniques. The working principle of the conceptual model of ambipolar transistor was confirmed through the fabrication of samples based on LOFET substrate. However, set of basic electrical properties obtained during the measurement and characterization stage in a clean-room environment, using the in-house developed probe station, have revealed certain issues connected with the fundamental behaviour of those fabricated devices, see Figure 5 further ahead for closer details. Despite the fact that both transfer characteristics suggest rather moderate ambipolar behaviour, especially mobility of charge carriers and ON/OFF ratio need to be further improved.

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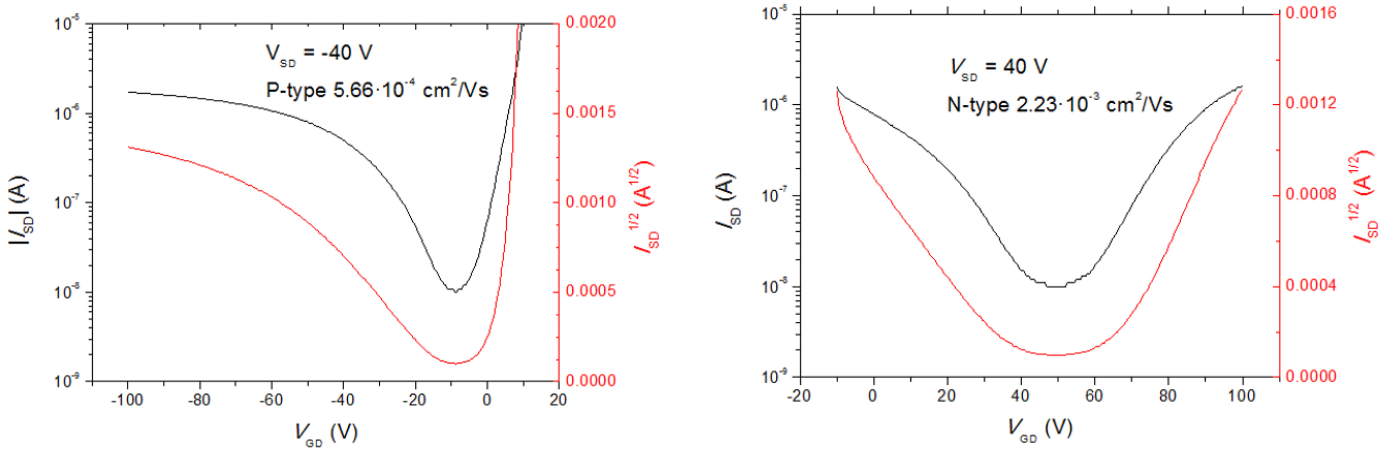

Fig. 5. The ambipolar characteristics of OFET devices fabricated with the mixture of Tips-Pentacene and PCBM-C60 compounds. Charge carriers mobility and transfer characteristics in both N- and P-conduction modes are shown, P-mode on the left and N-mode on the right.