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More Complex Polymorphic Circuits: A Way to Implementation of Smart Dependable Systems

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Abstract:
Today, there are a lot of application areas, where a circuit, which is able to perform different functions in different situations, may be useful. Typically, polymorphic circuits provide very area-efficient implementation and have also embedded and distributed sensing of an environment state. It might be a useful attribute to be considered for a dependable system design. This paper is dealing with a more complex polymorphic circuits with dependability feature and their physical implementation. The actual experimental setup was based around reconfigurable polymorphic chip REPOMO32 as a target environment, which is primarily designed to be configured (besides the configuration bit stream itself) by means of using the level of power supply voltage (V_{dd}). A part of polymorphic FIR filter was mapped onto the resources available inside REPOMO32 chip. Obtained results indicate feasibility of a full-scale implementation comprising several REPOMO32 chips.

INTRODUCTION

Nowadays, there undoubtedly exist diverse application areas, where a circuit, which is able to perform different functions in different situations, may be useful. Most simple approach is to design as many different circuits, as the overall number of functions that are actually needed. Then, outputs of these circuits are switched according to currently required function. This straightforward approach is perfectly functional, but quite ineffective in terms of the resulting implementation size. Another way to follow is reconfiguration. This perspective brings more area-efficient design and great flexibility – also circuits that were not prepared during design phase could be implemented (evolvable hardware), but may be less effective in terms of required time. Recent achievements in the field of digital design techniques and components of digital circuits provide yet another conception – so called polymorphic electronics. Polymorphic electronics as a research field was pioneered by Stoica et al. [1].

Typical polymorphic circuit is designed as a compact structure based around multifunctional components, where its structure remains unchanged during all operation modes while only the function of individual components changes. This ensures that polymorphic circuits are very area efficient in comparison to conventional multi-function circuits. Polymorphic circuits typically change their function in accordance with the state of an environment. The environment in this particular case is represented by a physical quantity that involves some parameters regularly used in connection with electronic structures – power supply voltage level, voltage level of a signal, temperature etc. [2] In certain applications it may be helpful to introduce new (better than existing) solutions [1][3][4]. Change of the circuit function comes immediately (with no delay introduced) and sensitivity to the external operating environment is seamlessly embedded to the target circuit. Today's applications are based on unipolar semiconductor transistors but the nature of polymorphic electronics is far more general. It is very important for future that the concept of polymorphic electronics is divided into technologically dependent (components, gates) and independent (synthesis techniques, applications) areas, because it could be also exploited with future emerging semiconductor technologies (e.g. carbon-based nanotechnology) [5][6]. But also with the available semiconductor technology (CMOS devices) the concept is ready to be applied and may offer some notable benefits to the area of multifunctional digital circuits [7].

Several polymorphic gates have been designed but only two were successfully manufactured so far; remaining polymorphic gates were either only simulated or tested in a field programmable transistor array (FPTA-2). For real experiments, the first reconfigurable polymorphic chip in the world was designed and physically fabricated. The chip is called REPOMO32 (REconfigurable POlymorphic MOdule with 32 configurable elements) [8]. The chip was tested extensively after manufacturing and its special capabilities were also used to demonstrate unique method of chip identification [9].

The paper presents almost first physical implementation of a more complex polymorphic circuit. Due to lack of physical implementations of polymorphic gates, only some simple polymorphic circuits were demonstrated so far [4][7]. Nowadays, the existence of a REPOMO32 chips enables us to actually implement and validate some previously proposed applications. In [10] a finite impulse response filters (FIR) was proposed, which are able to reduce their power consumption by reduction of

active stages (coefficients). Remaining stages of a filter are "reconfigured" (particularly, coefficients are changed) to achieve as much similar response (to the original filter), as is possible. Of course, the response of the reduced filter is not exactly the same; parameters of the reduced may show slightly worse behavior, but significant reduction of power consumption helps to mitigate these imperfections. Main goal of this paper is to clearly demonstrate feasibility of the approach where REPOMO32 modules could be used in order to implement the FIR filter functionality.

COMPONENTS FOR POLYMORPHIC CIRCUITS

As it was stated, one of main advantages of polymorphic electronics is efficiency in terms of size. To fulfill size-oriented constraints of a circuit, which exhibits more than one function with the same (unchanged) structure, components of the circuit have to be multi-functional and these components must be defined at the lowest possible level. Lower level means more size-efficient solution.
It implies that most size-efficient solution could be reached at the transistor level. Today components of polymorphic circuits (polymorphic gates) are designed at that level. But at the transistor level, the circuit behaves as an analogue circuit rather than digital. The transistor is not a pure digital component.
Thus, the lowest suitable level for the design (synthesis) of multifunctional (and also polymorphic) circuits is the gate level. Therefore, components of multifunctional (polymorphic) circuits are such gates, whose are able to exhibit more than one function.

Polymorphic gate is an element which performs an elementary logic (Boolean) function, whereas the function may (for the same element) vary in accordance with the particular state of the environment. It is possible to say that the function of the gate is virtually controlled by environment. Such feature may be useful for variety of applications and may save chip area and reduce global interconnections significantly.

Table 1 surveys the polymorphic gates reported in literature. For each polymorphic gate, the logic functions performed by the gate are given together with the values that represent recommended setting of the control signal variable. The number of transistors characterizes the size of polymorphic gates only partially as the transistors occupy different areas and the gates were fabricated using different fabrication technology.
Only two of the polymorphic gates have been fabricated so far; remaining polymorphic gates were either simulated or tested in a field programmable transistor array (FPTA-2). For instance, the 6-transistor NAND/NOR gate controlled by Vdd was fabricated in a 0.5-micron HP technology. Another NAND/NOR gate controlled by V_{dd} was utilized in the REPOMO32 chip. The gate is described in next section in more detail.

In 2010 Tanachutiwata et al. published some experiments with a device manufactured on graphene base (one atom thick layer of carbon). This device realizes several logic functions in accordance to voltage level on its electrodes [17]. For different voltage levels, differently polarized p-n junctions appear in the structure. Size of the device is comparable to a conventional 22 µm CMOS NAND gate. One of biggest advantage of graphene based devices is also speed. It seems that graphene may be perspective way to fulfill Moore's law after pure silicon devices and with the natural multifunctionality of graphene devices; conception of polymorphic electronics may be inspirational for future logic design.
Basic function of the device introduced in [17] is two-input multiplexer. However, table of possible functions of the device in [17] shows 8 functions in total. These functions could be reached by proper p-n junction polarization and utilization of electrodes. Seemingly the very simple device could exhibit a lot of functions, but in fixed connection of electrodes, two functions could be selected. So the device could be used as two-function polymorphic gate where the pair of functions exhibited by the gate could be selected by connection.

Existing Polymorphic Gates

Gate	*Control values*	*Controlled by*	*Transistors*
NAND/NOR	3.3/1.8 V	V_{dd}	6
AND/OR	1.2/3.3 V	V_{dd}	8
NAND/NOR	5/3.3 V	V_{dd}	8
AND/OR	27/125 C	temp.	6
AND/OR	5/90 C	temp.	8
NAND/NOR	0/5 V	ext. V	10
NAND/NOR	5/0 V	ext. V	8
NAND/NOR	5/0 V	ext. V	10
NAND/XOR	5/0 V	ext. V	9
AND/OR	0/3.3 V	ext. V	6
AND/OR/XOR	3.3/1.5/0 V	ext. V	9
NAND/NOR	0/5 V	ext. V	10

REPOMO32

NAND/NOR Polymorphic Gate

Mutual collaboration between research teams at Brno University of Technology (The Microelectronics Department at The Faculty of Electrical Engineering and Communication represented by Mr. Roman Prokop and The Faculty of Information Technology) has enabled the creation of polymorphic gate with two inputs, whose function is controlled by supply voltage [4]. The gate will accomplish two primary functions f1 and f2. Whereas f1 needs supply voltage

of at least 5 V in order to be executed correctly, function f2 demands lower supply voltage of 3,3 V which is still, however, quite typical for digital logic circuits. Particular logic functions to be performed were assigned in a following way: f1 = NAND a f2 = NOR.
The gate is composed of eight MOS transistors (3 n-MOS a 5 p-MOS). Structure of the gate is shown in Figure 1 (bottom-right). Common NAND or NOR gate built with CMOS technology contains exactly four transistors. The resulting size of the created polymorphic gate seems to be acceptable in this perspective – it has the same "price" as a pair of ordinary CMOS gates. Such finding can be also interpreted as if the polymorphic was replacing two usual gates in some class of applications. But if a pair of two standard gates (consisting of NAND and NOR gate) should replace the aforementioned polymorphic gate in functionally identical way, it would be necessary to append also detector of supply voltage level and some type of switch. The purpose of this switch would be then to select one of the two standard gates for the output according to the detected supply voltage level. Thus, it's easy to observe the overhead associated with conventional approach.

Structure of REPOMO32

REPOMO32 is primarily intended for implementation of polymorphic four-input/four-output combinational circuits. As Figure 1 shows, the chip consists of 32 two-input Configurable Logic Elements (CLEs) laid out in an array of 4 rows and 8 columns. A CLE can be programmed to perform one of the following functions: AND, OR, XOR and polymorphic NAND/NOR (described in previous section). When Vdd = 3.0–3.8 V, the NAND/NOR gate exhibits the NOR function and when Vdd = 3.9–5 V the gate exhibits the NAND function. If the CLE is set to exhibit one of ordinary logic functions, it do not change its logic functions with the changes of Vdd within the range of 3–5 V.
REPOMO32's logic behavior is defined by its configuration bits and the level of Vdd. The configuration bits control a set of multiplexers which are responsible for interconnecting the CLEs and selecting their logic functions. In total, 8 bits define the configuration of a single CLE. The configuration of the chip is stored in 32 8-bit latch registers. The configuration of a single CLE is performed by supplying CLE's address (addr) and configuration data (data) followed by activating the WE signal. The chip can be completely reconfigured in 32 configuration steps. The primary outputs Z0–Z3 are connected directly to CLEs of the last column. There are no synchronization registers in REPOMO32. The chip has 28 pins and occupies the area of 2900 x 1970 μm. It was fabricated using AMIS CMOS 0.7 μm technology. The REPOMO32 chip is considered as a small module which may be embedded into a larger system.

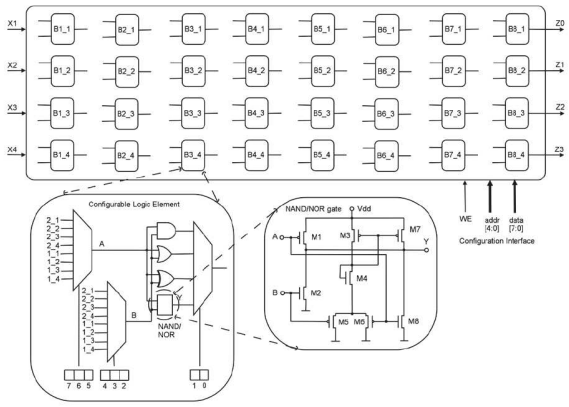

Fig. 1: The REPOMO32 chip, implementation details of the CLE block and NAND/NOR gate

DEPENDABLE APPLICATIONS

Stoica et al. mentioned in the pioneer work on polymorphic electronics [1] a range of potential applications. As the main advantage authors see a possibility of design such circuits, which have one main function and another additional function. This additional function (or functions) could be naturally activated under certain circumstances or on demand.

Stoica and his team also propose a polymorphic circuit, which works as a clock generator under normal circumstances. But when a special key is applied (e.g. certain temperature or some electromagnetic pulses, V_{dd} change, etc.), the circuit could generate a burst of pulses, which wakes up a special coding scheme [1]. Another application is able to utilize features of polymorphic electronics in such a way that a scanned fingerprint (or another biometric data) is converted to a matrix of voltages, which are then applied to different parts of a circuit. It causes enabling of the second (hidden) function of the circuit and the entire circuit works by another (intended) way. This allows to make a personalized chip with biometric data "wired" directly in silicon.

The article [1] also mentions a potential of the polymorphic electronics in dependable, fail-safe and adaptive applications. Additional functions could take the control over the device when the device may be in a danger. Polymorphic electronics enable to develop systems that adapt themselves very smartly and quickly to varying environment. This is possible due to the fact that no reconfiguration or rewiring is needed to change the function. And in contrary to multiplexing of several independent modules the polymorphic circuit is much more area-efficient.

Starecek et al. [12] propose a method for digital circuit testability improvement using polymorphic circuits. They show by experiments that if some gates in a circuit are replaced by polymorphic ones (without change anything in the structure), amount of

test patterns needed to test the circuit would be significantly reduced. When carefully selected gates are replaced by polymorphic gates with one of exhibited functions same as original gates, the circuit could work as original circuit in one mode and could be tested in another. The test will be shorter and cheaper. If polymorphic gates controlled by V_{dd} are employed, there is no need to complicate the structure with a global signal that indicates either working or test mode. The circuit could work with such V_{dd}, which ensures the mode of polymorphic gates equivalent to original gates. When a need of testing occurs, then the V_{dd} is simply changed to level on which polymorphic gates change their behavior and the test could start. Experiments show that it is possible to reach 30% reduction of test patterns amount needed to test the circuit; the test reduction is paid by slight increase of the occupied area.

Sekanina [13] have proposed several adders with self-testing property, which are able to indicate good or erroneous function on their carry outputs. The advantage of the approach is that no special output to indicate error is needed and the information about the error could propagate in ordinary circuit structure naturally without any special logic or additional signals. The proposed concept utilizes polymorphic gates with two possible functions. Under normal conditions (no error) outputs of the adder generate the same value for both modes of polymorphic gates. But when an error occurs, output value on the carry output of the adder differs for different modes of polymorphic gates. So the test of the circuit could be performed anytime by simple change of polymorphic gates function. If e.g. polymorphic gates controlled by V_{dd} are employed, the change of V_{dd} anytime is sufficient to perform the test.

Already A. Stoica et al. in their pioneer work on polymorphic electronics [1] propose an application in which an polymorphic AD converter is able to reduce data width and/or sample rate when a chip temperature arises or V_{dd} goes low to reduce power consumption and heat dissipation. This may prevent total collapse of a system in harsh environment and preserve at least most necessary functions. Ruzicka [7, 15] has proposed and experimentally verified application of polymorphic counters/ controllers. This application uses the circuit polymorphism for adoption of a system to varying environment such as falling of power supply voltage (a battery of an autonomous device goes low and sunset comes up so it is not possible to charge the battery using solar cells) or when temperature rises up (cooling system is not able to keep the device cool, e.g. outer temperature is high at the moment). But there is still an expectation of improvement in the future (the sunrise occur and solar cells loads the battery or outer temperature fall down). The device may be able to reduce its functionality under bad circumstances and restore it back when the environment goes better as smart as possible and the cost of such adaptability or fault-tolerance must be low. Polymorphic electronics is the technology that fulfills these requirements very well. Conventional solution would probably employ two modules (one for normal and one for emergency mode). Approach that employs reconfiguration has also significant overhead (comprises from configuration memory, control circuitry to load new configuration, configurable module with configurable elements and an interconnection network). There are two possible ways to create polymorphic sequential circuits. First is to propose polymorphic flip-flops as it was proposed by Stoica et al. [14]. But it is not easy to synthesize circuits with such flip-flops. There are no synthesis methods to design circuits with poly-functional flip-flops, perhaps evolutionary design may help. Another approach, proposed by Ruzicka, is based on employing of ordinary flip-flops and polymorphic gates in the next-state logic. Because there are several techniques to synthesize polymorphic combinational circuits [11, 16], design of sequential polymorphic circuits consisting ordinary flip-flops in combination with polymorphic gates is much more viable.

Sekanina, Gajda and Ruzicka propose also another dependable application of polymorphic electronics that reduces the power consumption in critical moments [10]. It is also signal processing application. Authors propose finite impulse response filters (FIR), which are able to reduce their power consumption by reduction of stages (coefficients). Remaining stages of a filter are "reconfigured" (particularly, coefficients are changed) to achieve as much similar response (to the original filter), as is possible. Of course, the response of the reduced filter is not exactly the same; parameters of the reduced filters could be slightly worse, but significant reduction of power consumption helps to overcome bad times.

POLYMORPHIC FIR FILTER

Figure 2 shows a polymorphic FIR filter, proposed in [10]. The filter consists of $N - 1$ delay registers, N multiplication units and an N-operand adder which is divided into two sub-adders whose outputs are summed in the third adder. The filter can operate either in the standard mode or backup mode. The standard mode is used during normal operational conditions of the filter. In that case, the filter is operated as any conventionally created N-tap filter with coefficients b_0–b_{N-1}. In the backup mode, the filter approximates the standard mode using restricted resources. In this mode the filter utilizes only M, where $M < N$ coefficients (b^*_0 –b^*_{M-1}) and $M - 1$ delay registers. Therefore, in the backup mode, original coefficient values b_0–b_{M-1} are reconfigured and unused parts of the filter are disconnected. To reconfigure coefficients, a polymorphic constant

multipliers could be used. The mode can be controlled by using either a logic signal (c in Figure 2) or V_{dd} level. If the polymorphic gates are controlled using V_{dd} and unused taps can be disconnected simply by changing V_{dd}, the control signal c is not required and the filter mode can be distinguished by the level of V_{dd}.

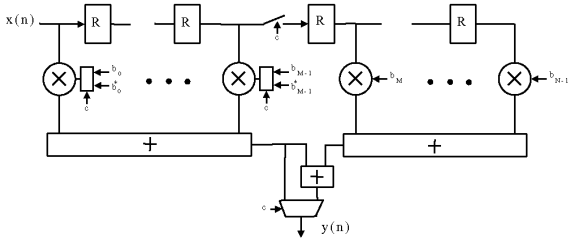

Fig. 2: Circuit Structure of Polymorphic FIR Filter

Constant Multipliers

Circuits calculating b_i x x in the standard mode and b^*_i x x in the backup mode are implemented using polymorphic and ordinary gates. In addition to ordinary gates, it contains only the polymorphic NAND/NOR gates because only these gates are available in REPOMO32. Figure 3 shows a part of one of them which calculates 240 x x / 32 x x. In the figure, the mapping of the circuit to one REPOMO32 chip is shown (compare to the vacant REPOMO32 structure in Figure 1). CLEs configured as polymorphic are violet ones. Note that outputs y_0–y_3 are always 0 (first "valid" output bit is y_4), outputs called "AUX" are internal signals of the multiplier, they are used for interconnection among other REPOMO32 modules.

Polymorphic Multiplexer

Also a final multiplexer, which selects between N-tap filter in the standard mode and M-tap filter in the backup mode, could be implemented as a polymorphic circuit. Its circuit structure is described in [11]. If employed polymorphic gates are in the NAND mode, data from A input are passed to the output, for NOR mode, data from B are passed to the output. If used polymorphic gates are V_{dd} sensitive and the multiplexer used at the output of proposed filter (see Figure 2), the mode of the filter (standard/backup) could be controlled by V_{dd}.

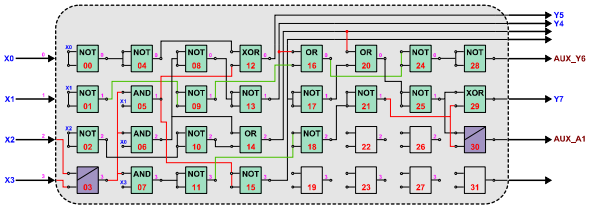

Fig. 3: Part of 240x/32x Polymorphic Constant Multiplier Implemented in REPOMO32

EXPERIMENTAL RESULTS

Main intention behind the experimental activities was to put together configuration of REPOMO32 shown on Figure 3, which represents an example of more complex circuit based around combination of conventional and polymorphic gates, and subsequently evaluate its functional properties when deployed into a real chip.

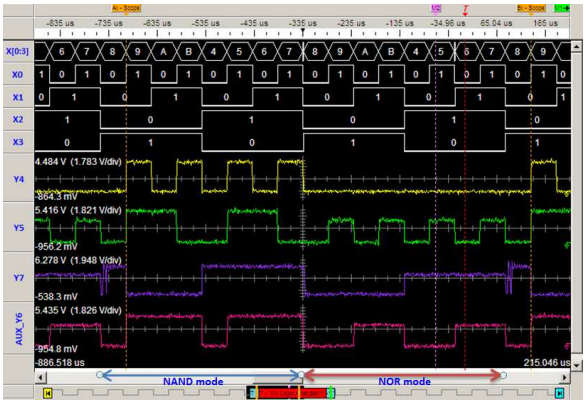

Fig. 4: Circuit Structure of Polymorphic FIR Filter

Signal waveforms depicted on Figure 4 document the behavior of the target circuit. Input stimulus is in this case represented by the signals denoted as *x[0:3]*. For better illustration of polymorphic properties the output signals *y4*, y5, *y7* and *aux_y6* are shown through analog waveforms. One can observe alternation of logic values 1 and 0 within the portion of signal trace that belongs to *y4* where NAND operation mode is active under supply voltage of 5V. Then, circuit enters NOR operating mode with transition of supply voltage to 3.3V and, therefore, signal *y4* hold 0V amplitude till the end of current computational cycle. These two operating modes can be distinguished in even better way when analyzing amplitudes of the remaining signals, for example *y5*.

CONCLUSIONS

Polymorphic electronics is possible approach to create multifunctional logic circuits with embedded sensing of an environment variable (e.g. V_{dd}). Some application areas were previously proposed, where these features bring benefits to the design and implementation of a circuit. One of these areas is the design of smartly dependable circuits. In this paper, one such application is demonstrated – a polymorphic FIR filter implemented using available reconfigurable polymorphic chips. The results obtained throughout experimental implementation followed by its analysis have undoubtedly confirmed the implementation feasibility of the initial theoretical concept behind polymorphic FIR filter. Combination of several REPOMO32 chips would finally allow the whole

filter to be realized. It's evident that even complex circuit structures of this nature can be successfully mapped onto the relatively constrained resources available in REPOMO32. Advantages of polymorphic electronics were also demonstrated here on a real example. It is very important for future that the concept of polymorphic electronics is divided into technologically dependent (components) and independent (synthesis techniques, applications) areas, because it could be usable also with future semiconductor technologies (e.g. carbon-based nanotechnology). But also with today's semiconductor technology (CMOS devices) the concept is ready to apply and may offer some benefits to the area of multifunctional digital circuits.

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REFERENCES

[1] Stoica, A., Zebulum, R. S., Keymeulen, D.: Polymorphic electronics. Proc. of Evolvable Systems: From Biology to Hardware Conference, volume 2210 of LNCS, Springer 2001, pp. 291–302.

[2] Růžička, R., Šimek, V., Sekanina, L.: Behavior of CMOS Polymorphic Circuits in High Temperature Environment. Proceedings of the 2011 IEEE Symposium on Design and Diagnostics of Electronic Circuits and Systems, IEEE CS, 2011, pp. 447 –452.

[3] Stoica, A., Zebulum, R. S., Guo, X. et al.: Taking evolutionary circuit design from experimentation to implementation: Some useful techniques and a silicon demonstration. IEE Proc.-Comp. Digit. Tech., 151(4), 2004, pp. 295 – 300.

[4] Růžička, R., Sekanina, L., Prokop, R.: Physical demonstration of Polymorphic Self-checking Circuits. Proc. of the 14th IEEE IOLTS, IEEE CS, 2008, pp. 31 – 36.

[5] Tanachutiwat, S., Lee, J. U., Wang, W., Sung, C. Y.: Reconfigurable multi-function logic based on graphene P-N junctions. Proc. of DAC 2010, pp. 883 – 888.

[6] Růžička, R., Šimek, V.: Polymeric Polymorphic Electronics: Towards Multifunctional Logic Elements Based on Organic Semiconductor Materials, In: Proceedings of CSE 2012, Košice, SK, FEI TU Košice, 2012, pp. 154-161.

[7] Růžička, R.: Gracefully Degrading Circuit Controllers Based on Polytronics. Proc. of 13th Euromicro Conference on Digital System Design, IEEE CS, 2010, pp. 809 – 812.

[8] Sekanina, L., Růžička, R., Vašíček, Z., Prokop, R., Fujcik, L.: REPOMO32 - New Reconfigurable Polymorphic Integrated Circuit for Adaptive Hardware. Proc. of the 2009 IEEE Symposium Series on Computational Intelligence - Workshop on Evolvable and Adaptive Hardware, Nashville, IEEE CIS, 2009, pp. 39 – 46.

[9] Sekanina, L., Růžička, R., Vašíček, Z., Šimek, V., Hanáček, P.: Implementing a Unique Chip ID on a Reconfigurable Polymorphic Circuit, In: Information Technology And Control, 42(1), 2013, pp. 7-14.

[10] Sekanina, L., Růžička, R., Gajda, Z.: Polymorphic FIR filters with backup mode enabling power savings. In 2009 NASA/ESA Conf. on AHS, IEEE, 2009, pp. 43–50.

[11] Gajda, Z., Sekanina, L.: On Evolutionary Synthesis of Compact Polymorphic Combinational Circuits, In: Journal of Multiple-Valued Logic and Soft Computing, roč. 17, č. 6, 2011, Philadelphia, US, pp. 607-631.

[12] Sekanina, L., Stareček, L., Kotásek, Z., Gajda, Z.: Polymorphic Gates in Design and Test of Digital Circuits. International Journal of Unconventional Computing, 4(2), 2008, Philadelphia, pp. 125 – 142, ISSN 1548-7199.

[13] Sekanina, L.: Evolution of Polymorphic Self-Checking Circuits. Proc. of Evolvable Systems: From Biology to Hardware, Berlin, Springer, 2007, pp. 186 – 197.

[14] Zebulum, R. S., Stoica, A.: Ripple Counters Controlled by Analog Voltage. NASA Tech Briefs, 30(3):2, 2006.

[15] Růžička, R.: Dependable Controller Design using Polymorphic Counters. Proc. of 12th Euromicro Conference on Digital System Design, Los Alamitos, IEEE CS, 2009, pp 355 – 362.

[16] Gajda, Z., Sekanina, L.: Reducing the Number of Transistors in Digital Circuits Using Gate-Level Evolutionary Design. 2007 Genetic and Evolutionary Computation Conference, New York, ACM, 2007, pp. 245 – 252.

[17] Tanachutiwat, S., Lee, J. U., Wang, W., Sung, C. Y.: Reconfigurable multi-function logic based on graphene P-N junctions. Proc. of DAC 2010, pp. 883 – 888.