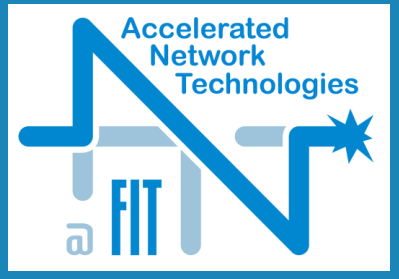
Precise IPv4/IPv6 Packet Generator Based on NetCOPE Platform



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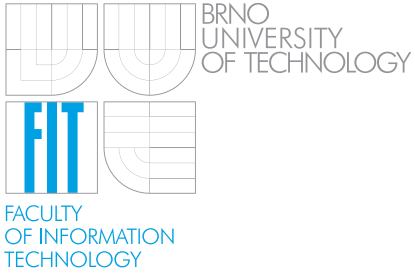


INVESTMENTS IN EDUCATION DEVELOPMENT

Outline

Motivation

- testing of network devices at speed of 10 Gbit/s
- existing but expensive special hardware network testers
- existing the NetCOPE platform for building hardware accelerated network applications

Software based solutions

- pros
  - availability of required sotware and hardware
  - well-known software tools (e. g. `tcpdump` and `tcpreplay`)
- cons
  - low throughput
  - inaccurate for time critical experiments

Hardware network testers

- pros
  - ability to operate at full wire speed
  - great number of possible settings
- cons
  - very high price

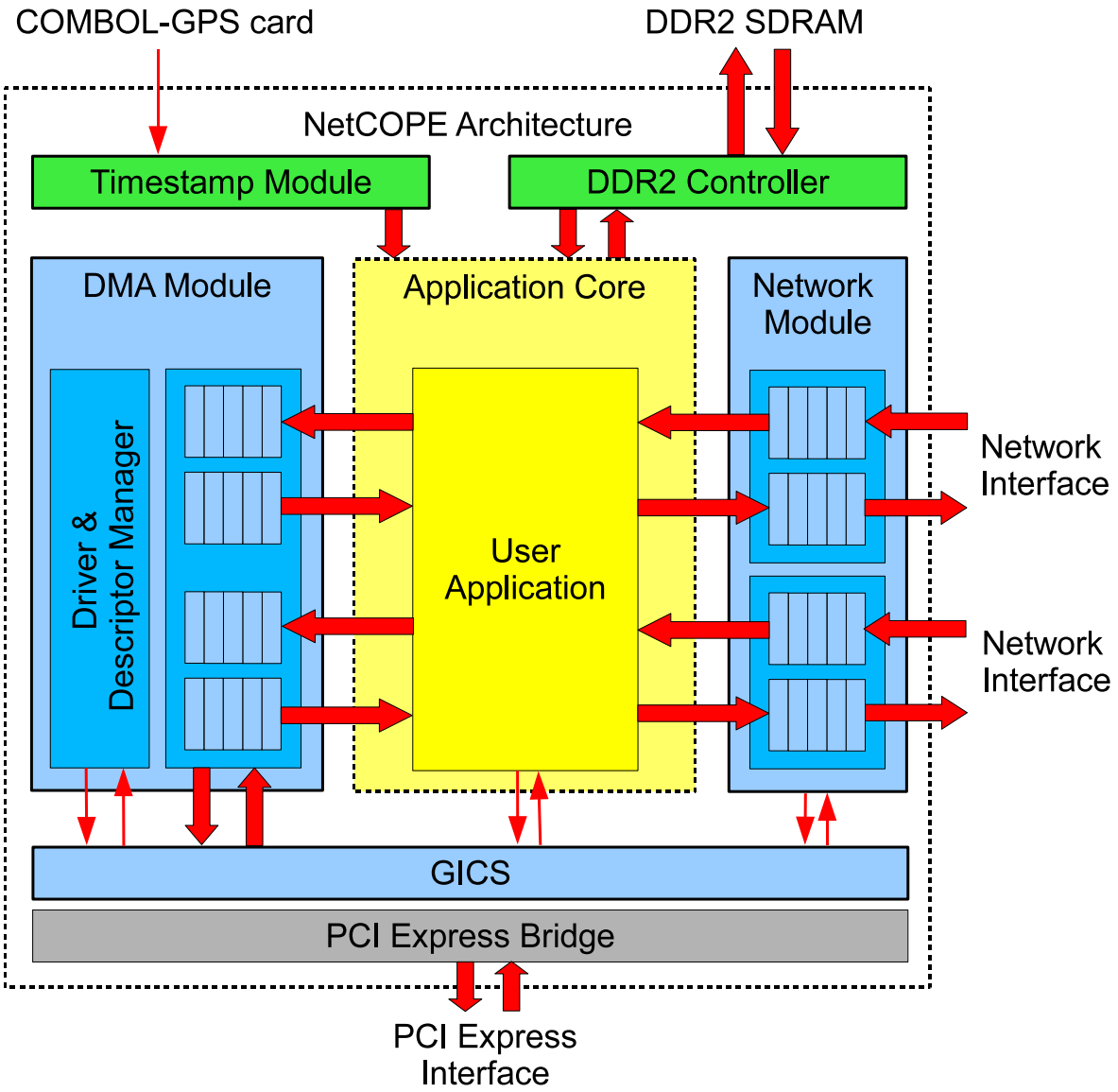
NetFPGA platform solution

- hardware card with the Virtex-II Pro FPGA chip developed at Stanford University
  - PCI bus connector
  - on-board memory (at most 64 MB)
  - four 1 Gbit/s network interfaces
- two stage transmission process
  - loading network traffic to the platform's memory
  - transmission of traffic from the memory
- pros
  - cheaper than hardware network testers
- cons
  - unable to operate at speed of 10 Gbit/s

COMBOv2 Cards

- **mother card** (Virtex-5 FPGA chip, PCI Express x8 interface, DDR2 SODIMM connector for up to 2 GB memory)
- **add-on cards** (2x10 Gbit/s or 4x1 Gbit/s interface cards, GPS-based clock system card)

NetCOPE Platform

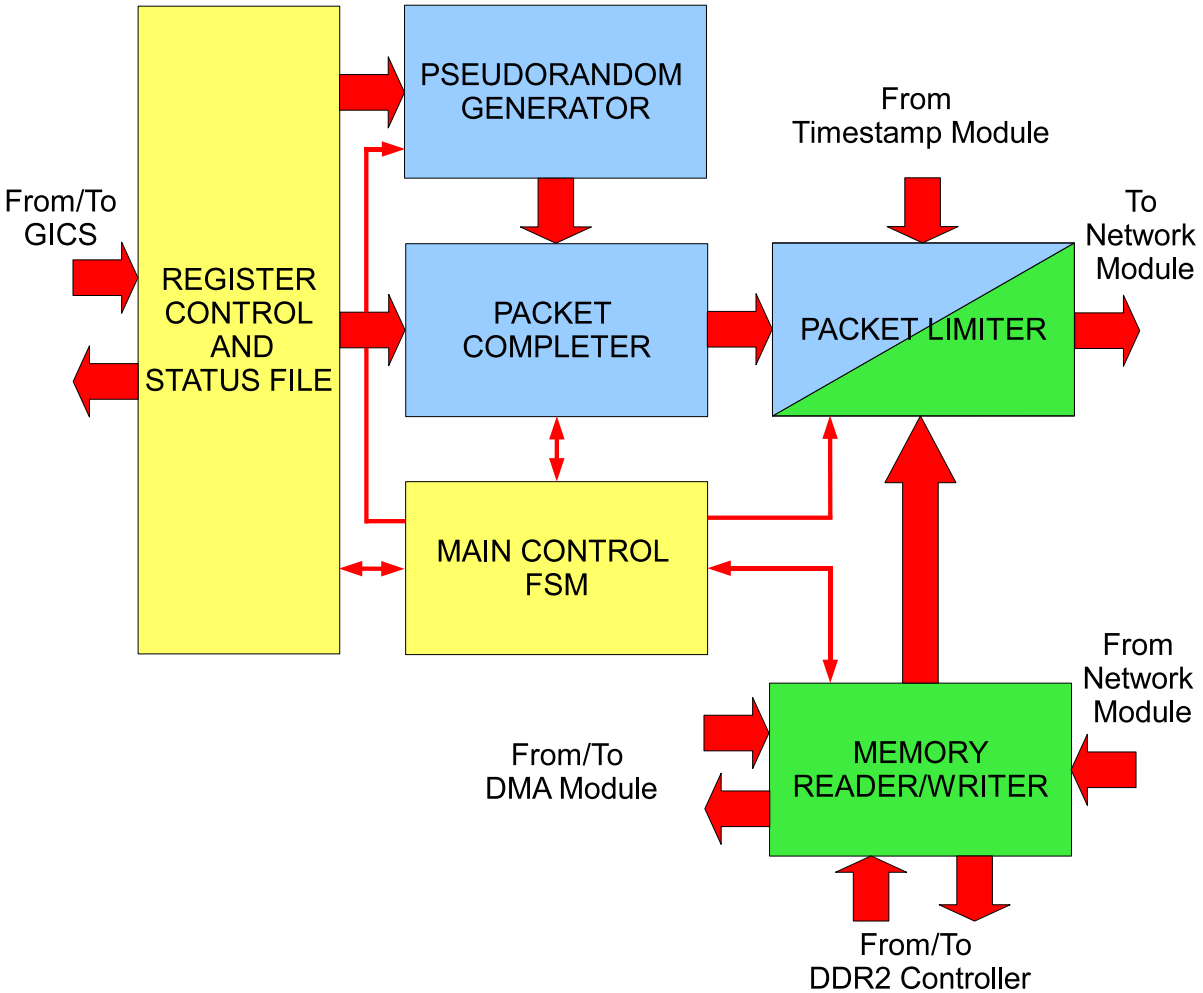


basic NetCOPE modules

expansion NetCOPE modules

user application

Generator Architecture



controlling operation

generating traffic

replaying traffic

Generator Submodules

Pseudorandom Generator

- generates IPv4/IPv6 header fields
- based on Multiple LFSR architecture

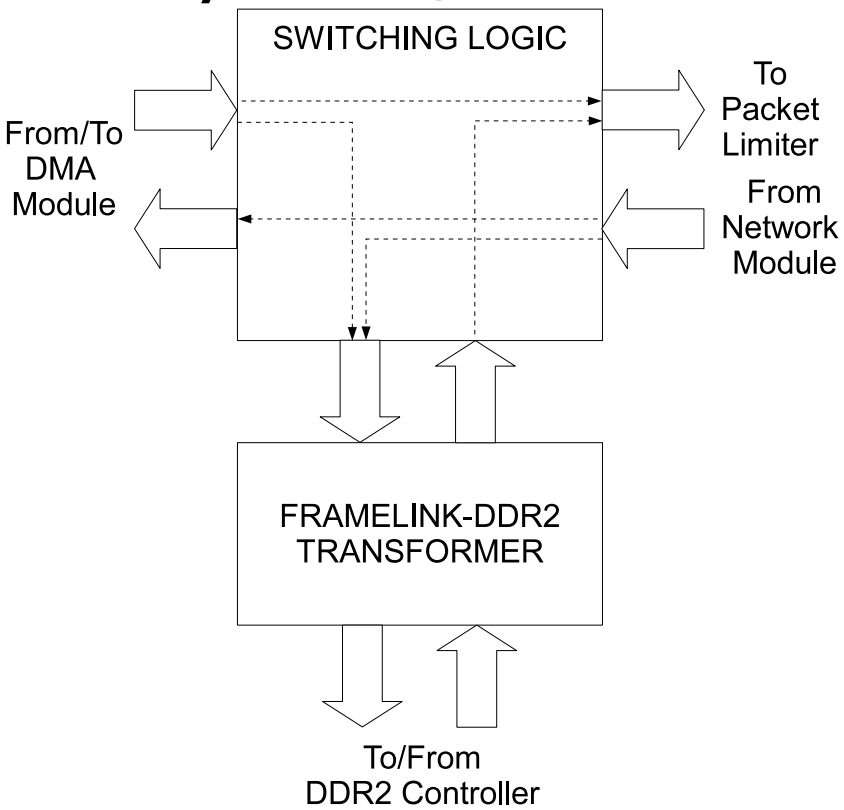
Generator Type	Diehard Score
LFSR	756
MLFSR	154
true	22

- utilizes DSP48 slices for shifting and multiplication

Packet Completer

- forms complete IP packet
- header fields can be generated or constant
- payload length can be generated or constant

Memory Reader/Writer



Packet Limiter

- plans and controls data transmission
- modes of data transmission limitation
  - no restrictions
  - limitation to specified bitrate
  - timestamp based limitation

Generator Submodules

Main Control FSM

- controls operation of all generator modules
- four different modes of operation
  - generating synthetic network traffic
  - loading data to the DDR2 memory
  - transmission data from the DDR2 memory
  - standard NIC

Register Control and Status File

- software accessible registers for controlling and monitoring generator's operation
  - registers for pseudorandom generator
  - mode of operation registers
  - IP protocol version
  - type of transmission limitation
  - etc.

Key Features

- 10 Gigabit Ethernet support
- synthetic network traffic generation
- DRAM based network traffic replaying
- software based network traffic replaying
- IPv6 support
- output rate limitation
- timestamp based transmission

Thank you for your attention