



## Packet Classification at wire-speeds

Packet classification is one of the basic steps in providing network security, enabling traffic policing, QoS provisioning, reliable transfers in VPN networks performed in network devices like firewalls or routers. Given a set of rules the goal is to find a best-matching rule to the header fields of incoming packets. Since classification involves many header fields, finding an algorithmic solution providing a wire-speed performance and acceptable memory requirements has achieved a great deal of interest in research community.

One of the promising techniques to cope with this problem is decomposition where classification is performed in several steps. The first is Longest Prefix Match done independently for every involved header field. The second is a mapping of the LPM results to the existing rule number. Using a perfect hashing approach for such a mapping it is possible to ensure fixed number of memory accesses and thus achieve constant time complexity which is essential for network security devices.

Data width	Croosproduct Based	Bloom Filter Based			Perfect Hash
		4	6	8	
9	37,5	9,38	1.00	4,6875	150
18	75	18,75	12.1	9,3750	150
36	150	37,50	25	18,7500	150
72	350	75,00	50	37,5000	150

Table 1: Throughput in millions of packets per second for given bus data widths for 300 MHz DDR memory and rule width of 144 bits.

The throughput is compared to other crossproduct-based techniques and according to the obtained results it is fully competitive approach to recently published algorithms.

### Perfect Hashing Crossproduct Algorithm for classification:

- provides wire-speed throughput independent of ruleset complexity
- significantly reduces memory resources using a hashing
- allows easy implementation in hardware
- is fully competitive to the other high-performance classification

### Published papers:

V. Puš, J. Kořenek., Fast and Scalable Packet Classification Using Perfect Hash Functions, FPGA '09: Proceedings of the 17th international ACM/SIGDA symposium on Field programmable gate arrays. Monterey, California, USA, 2009.

