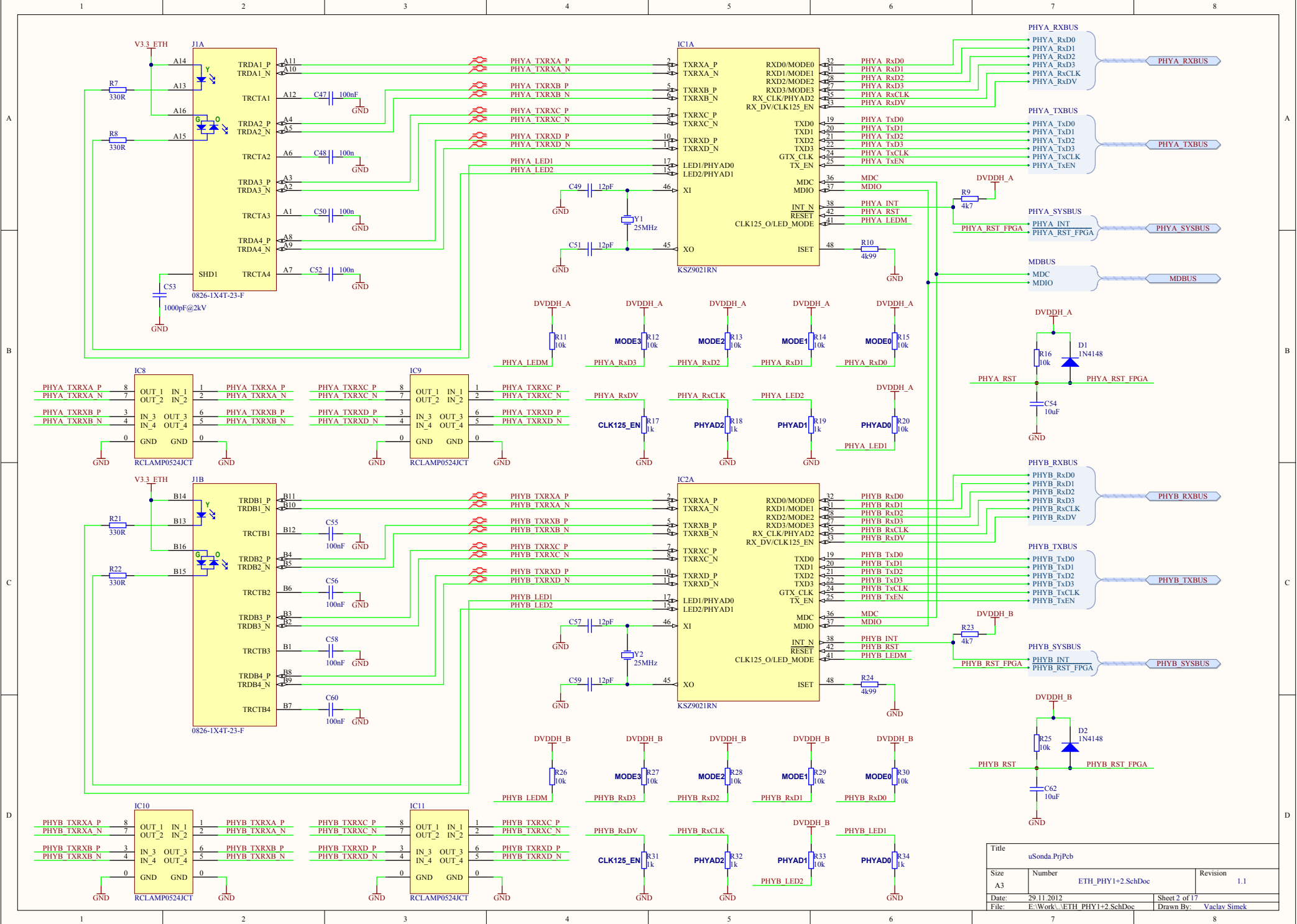
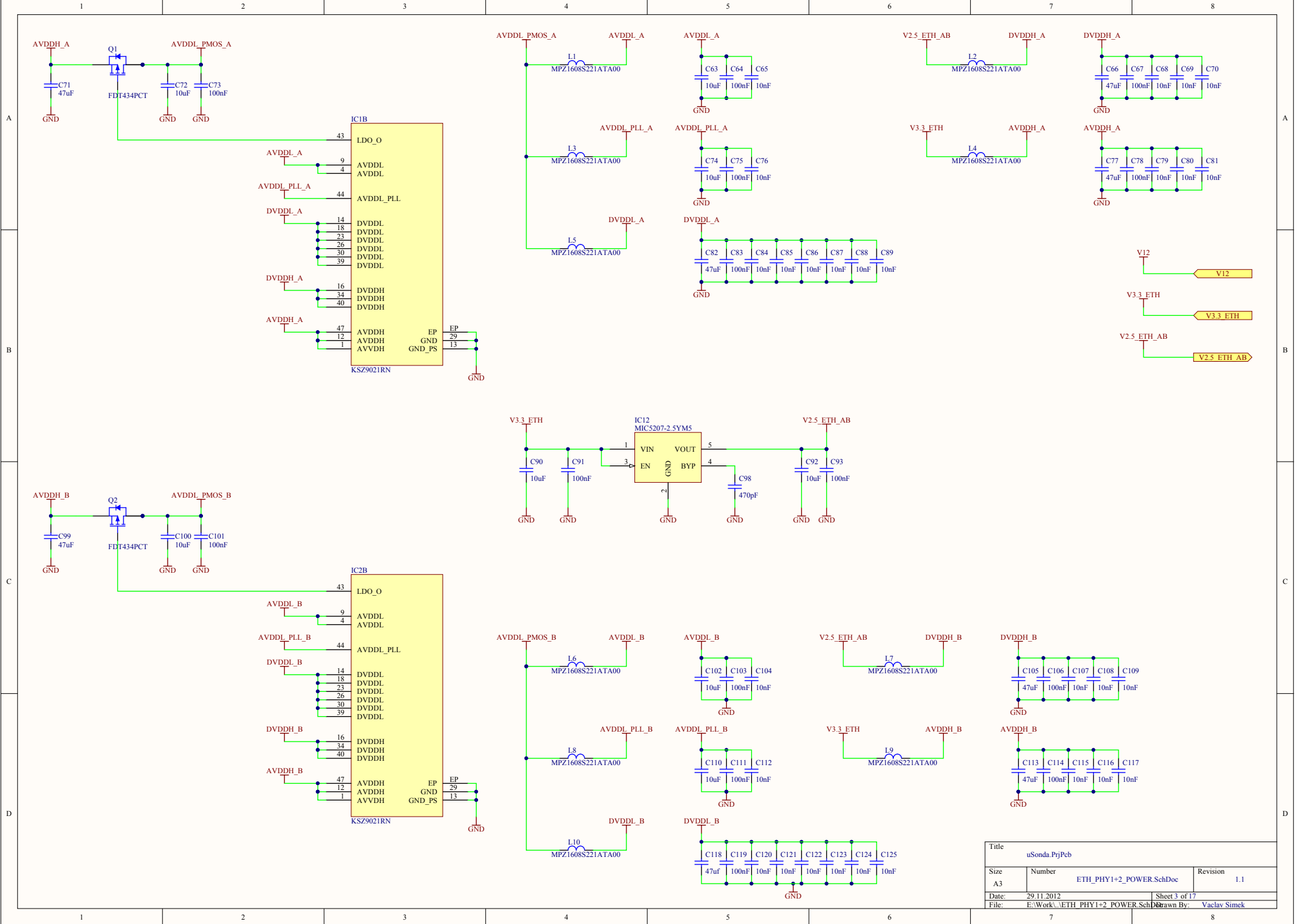


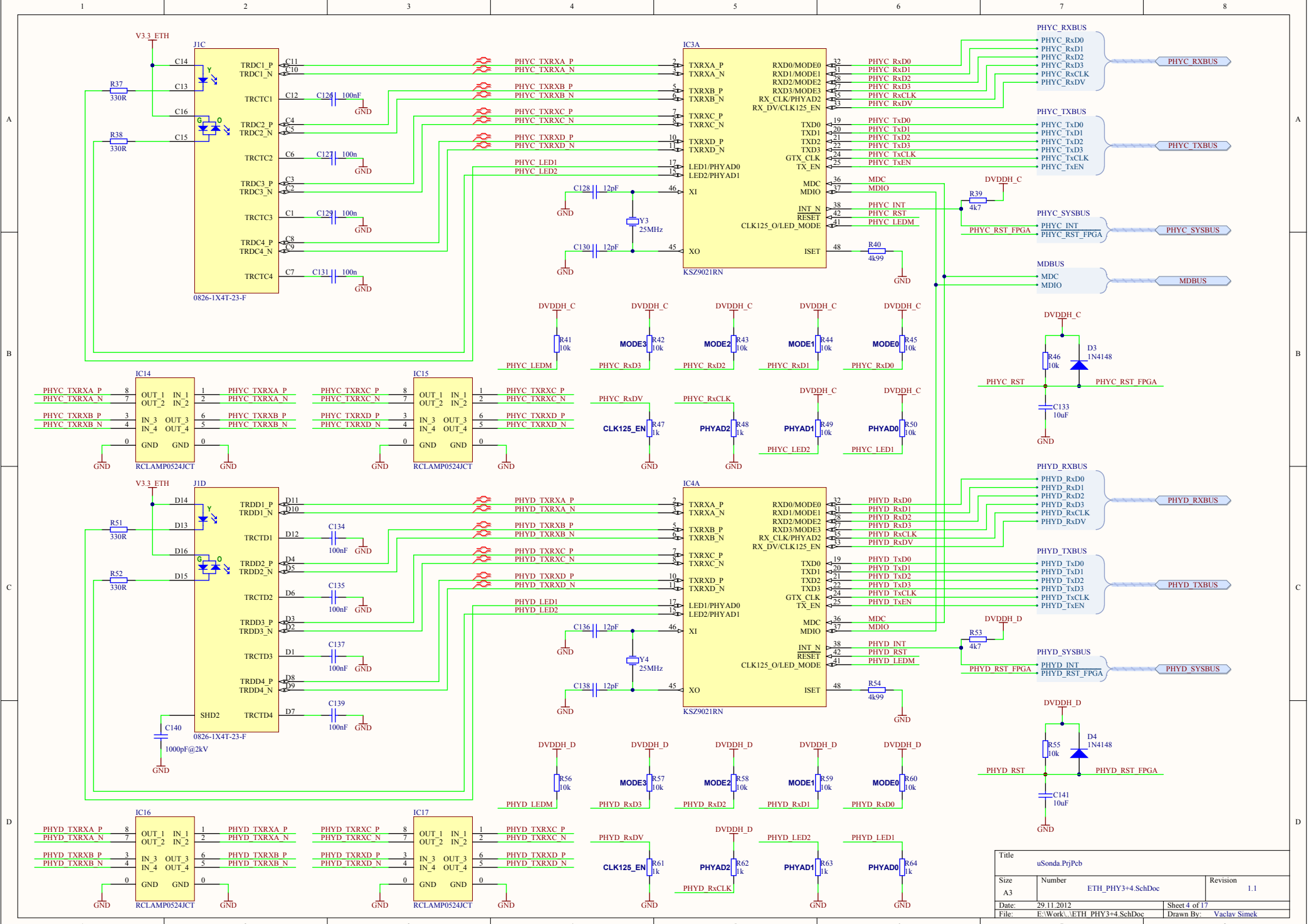
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uSonda.PrjPeb			
Size	Number	Revision	
A3	uSonda.SchDoc	1.1	
Date:	29.11.2012	Sheet 1 of 17	
File:	E:\Work\...uSonda.SchDoc	Drawn By: Vaclav Simek	



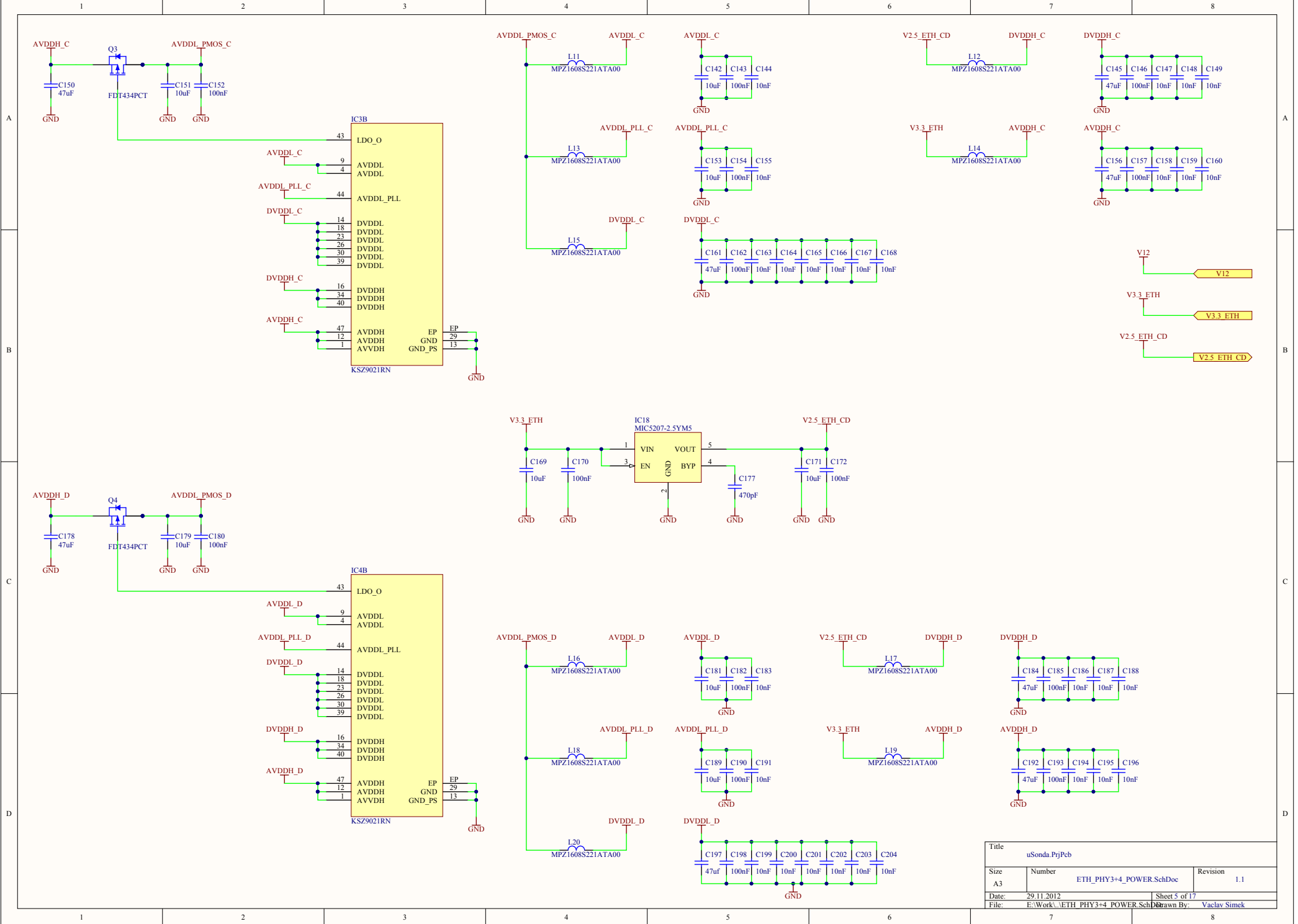
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Date:	29.11.2012		Sheet 2 of 17				
File:	E:\Work\...ETH_PHY1+2.SchDoc		Drawn By:		Vaclav Simek		



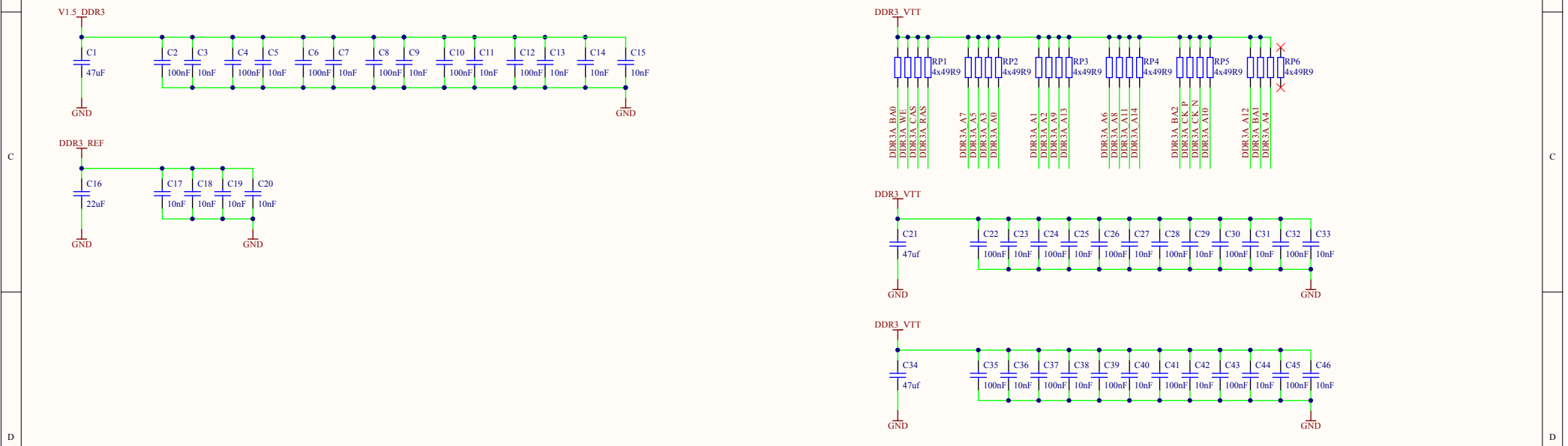
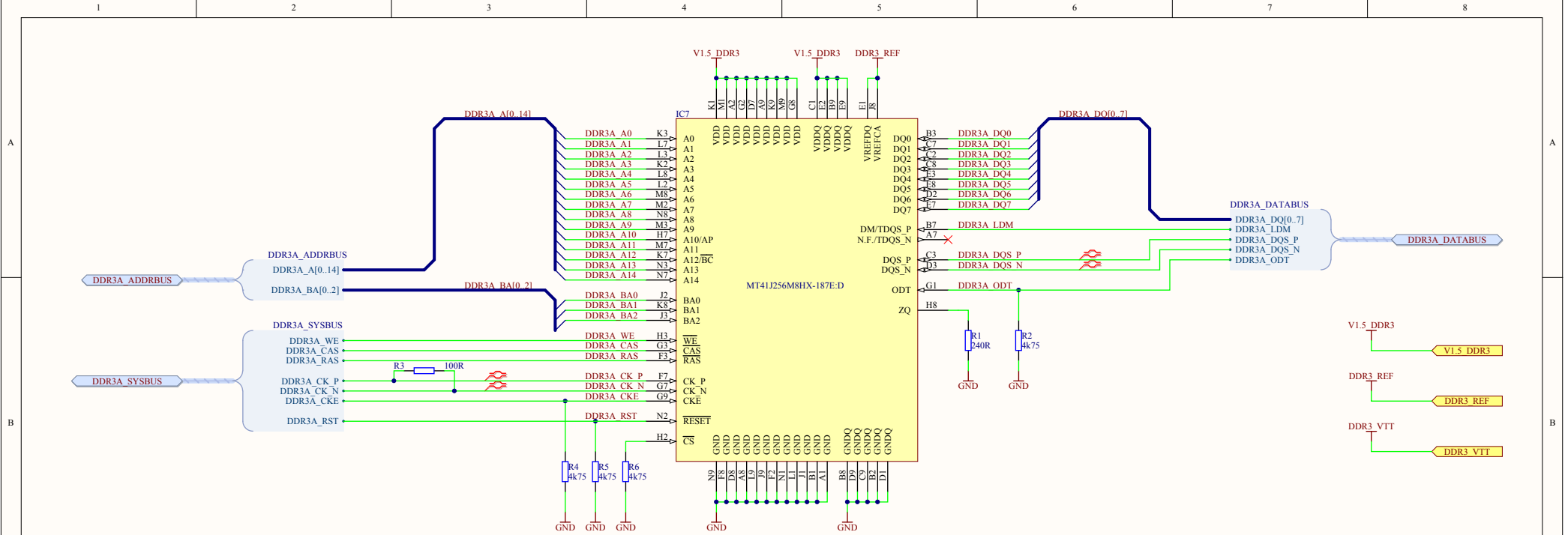
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Size	Number	Revision			
A3	ETH_PHY1+2_POWER.SchDoc	1.1			
Date:	29.11.2012	Sheet 3 of 17			
File:	E:\Work\...ETH_PHY1+2_POWER.SchDoc	Drawn By:		Vaclav Simek	



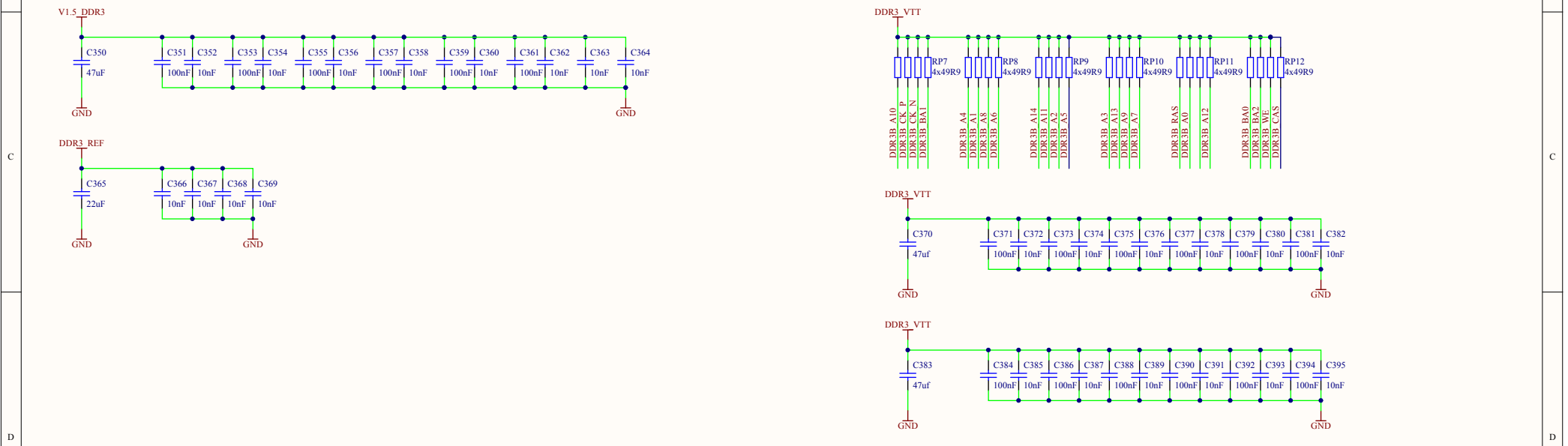
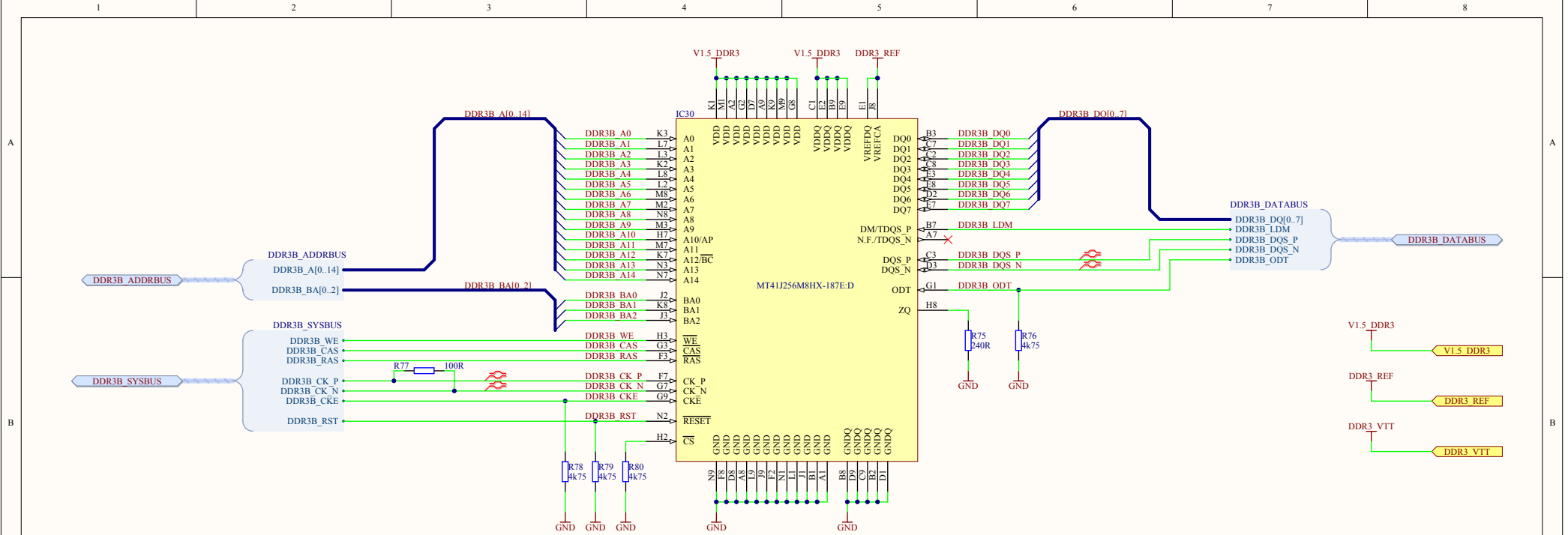
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Date:	29.11.2012	Sheet 4 of 17			
File:	E:\Work\ETH_PHY3+4.SchDoc	Drawn By:		Vaclav Simek	



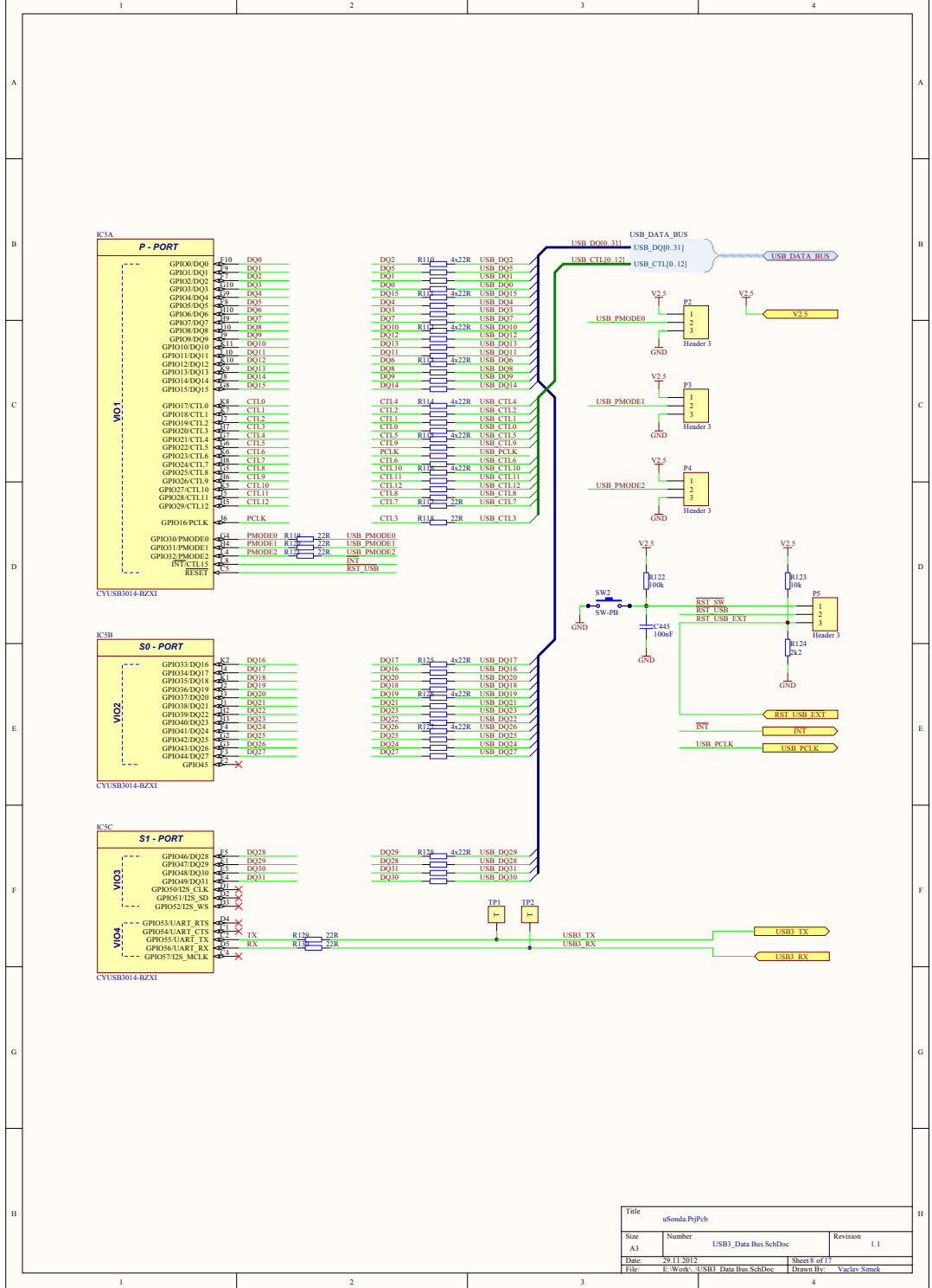
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Size	Number	Revision			
A3	ETH_PHY3+4_POWER.SchDoc	1.1			
Date:	29.11.2012	Sheet 5 of 17			
File:	E:\Work\...ETH_PHY3+4_POWER.SchDoc	Drawn By:		Vaclav Simek	



Title			uSonda.PrjPeb		
Size	Number	Revision			
A3	DDR3 Memory 1.SchDoc	1.1			
Date:	29.11.2012	Sheet 6 of 17			
File:	E:\Work\DDR3 Memory 1.SchDoc	Drawn By:		Vaclav Simek	

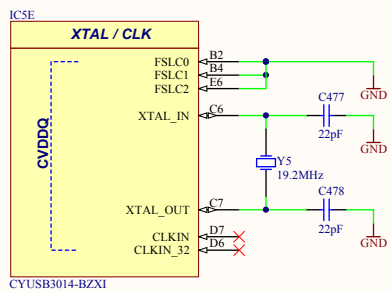
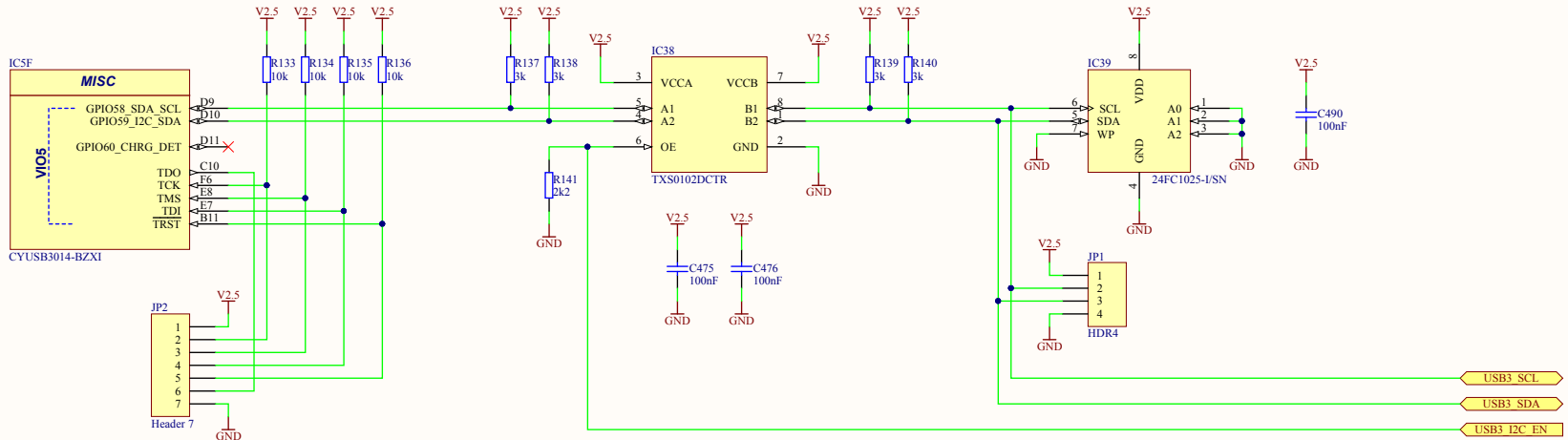
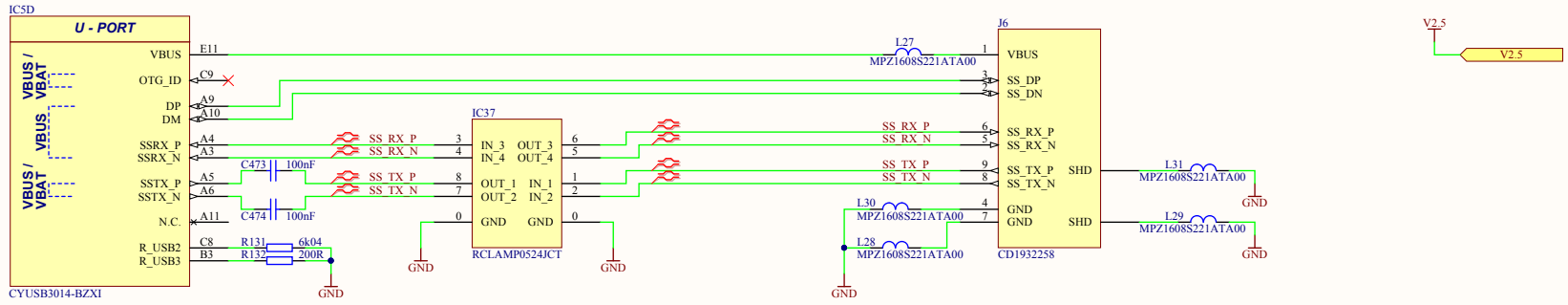


Title			uSonda.PrjPeb		
Size	Number	Revision		1.1	
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Date:	29.11.2012	Sheet 7 of 17			
File:	E:\Work\DDR3 Memory 2.SchDoc	Drawn By:		Vaclav Simek	

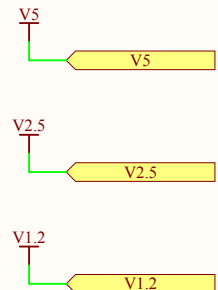
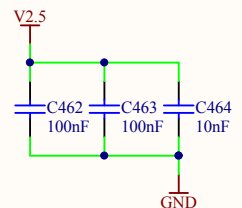
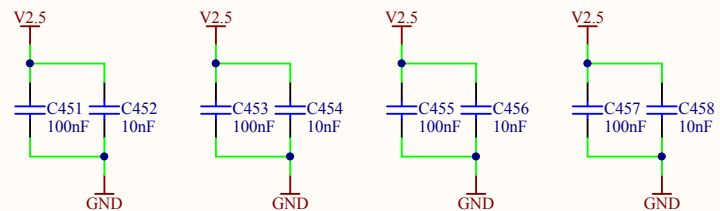
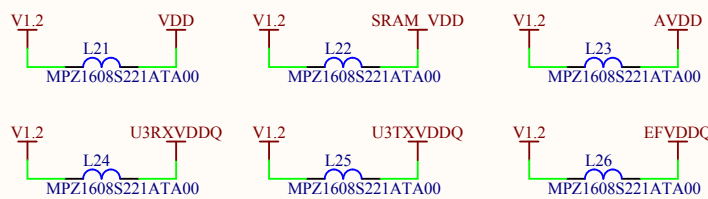
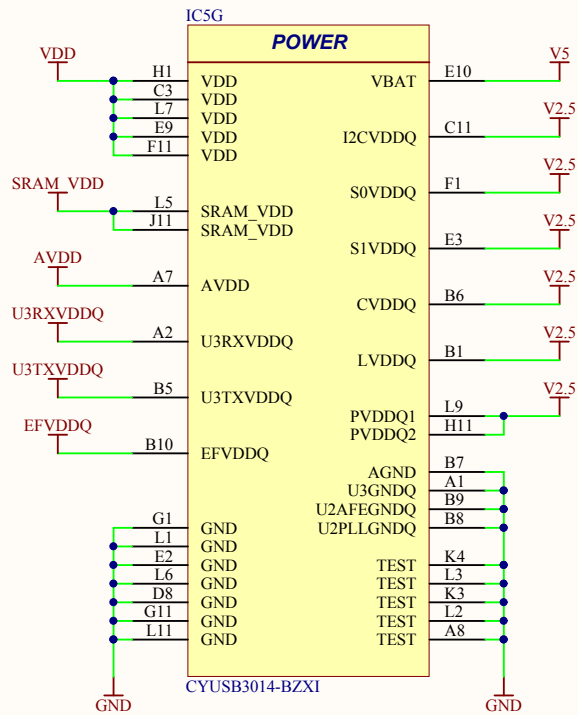
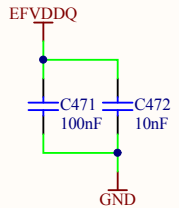
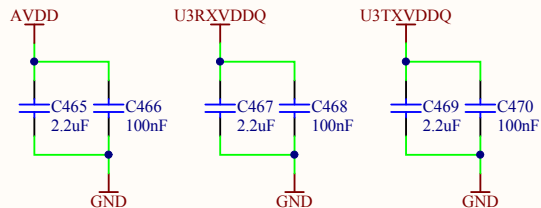
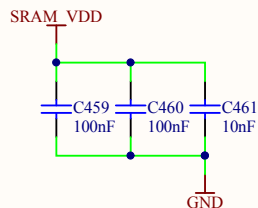
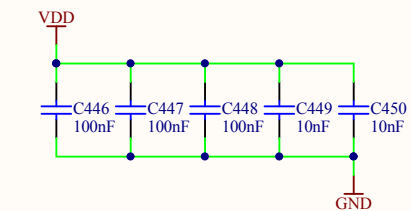


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aSomda PjPcb			
Size	Number	USB_Data Bus Sch.Doc	Revision
A3			1.1
Date	Sheet 8 of 1		
File	F:\Work\USB_Data Bus Sch.Doc	Drawn By:	Vadlav Suresh

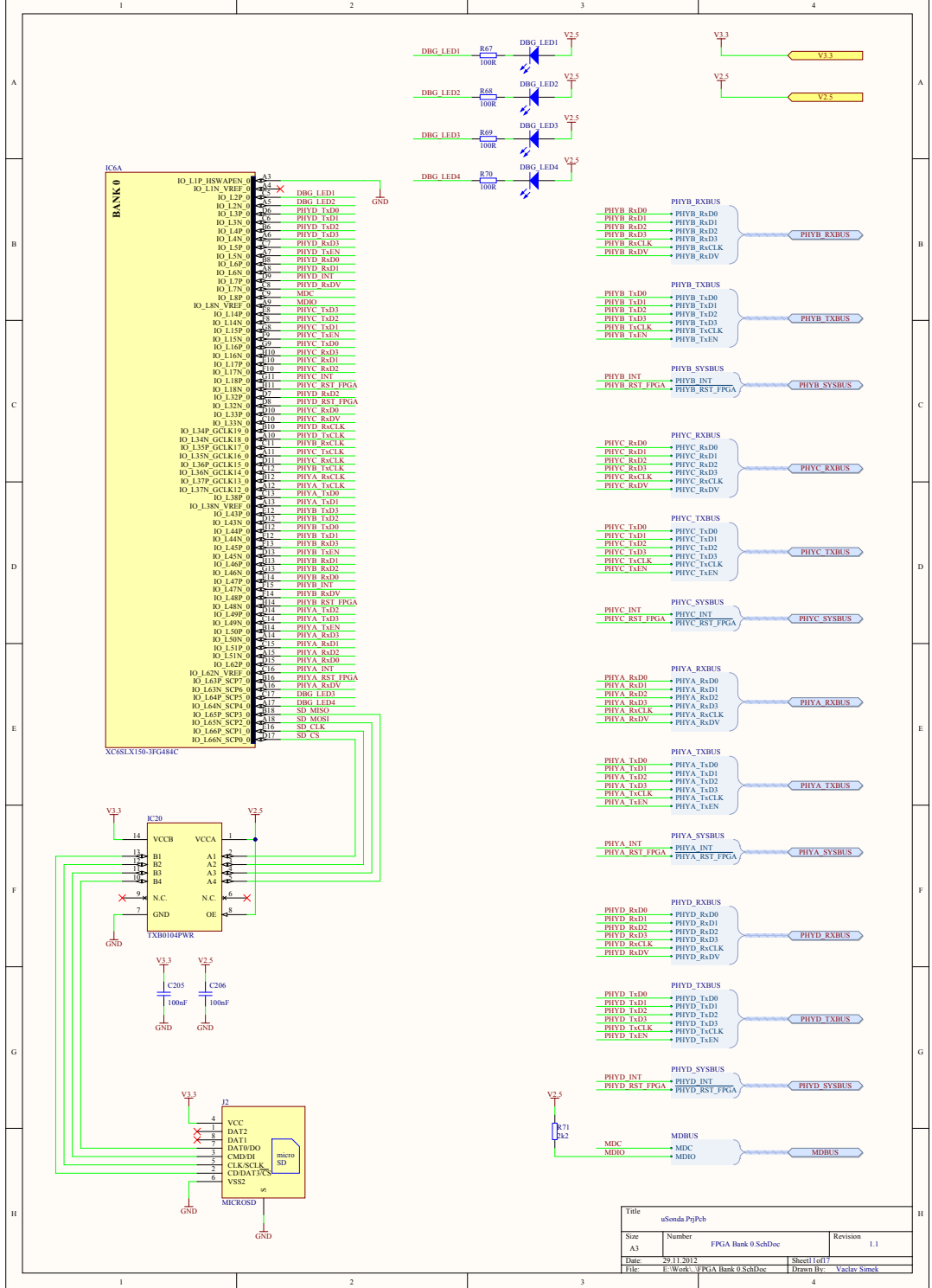




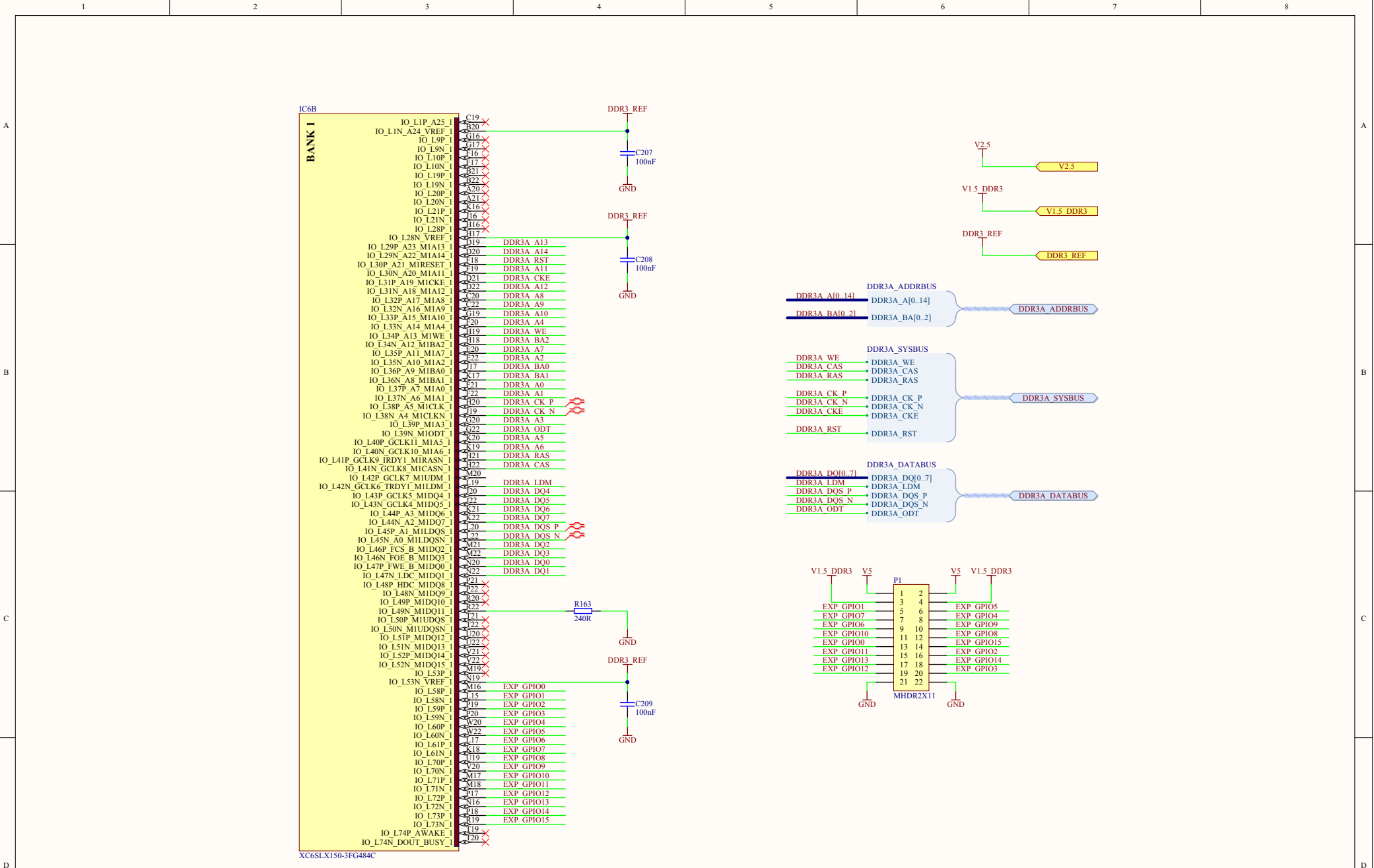
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Size	Number	Revision
A3	USB3_System Connections.SchDoc	1.1
Date:	29.11.2012	Sheet 9 of 17
File:	E:\Work\USB3_System Connections.SchDoc	Drawn By: Vaclav Simek



Title			uSonda.PrjPeb		
Size	Number	Revision			
A4	USB3_Power.SchDoc	1.1			
Date:	29.11.2012	Sheet	0 of 7		
File:	E:\Work\...\USB3_Power.SchDoc	Drawn By:	Vaclav Simek		

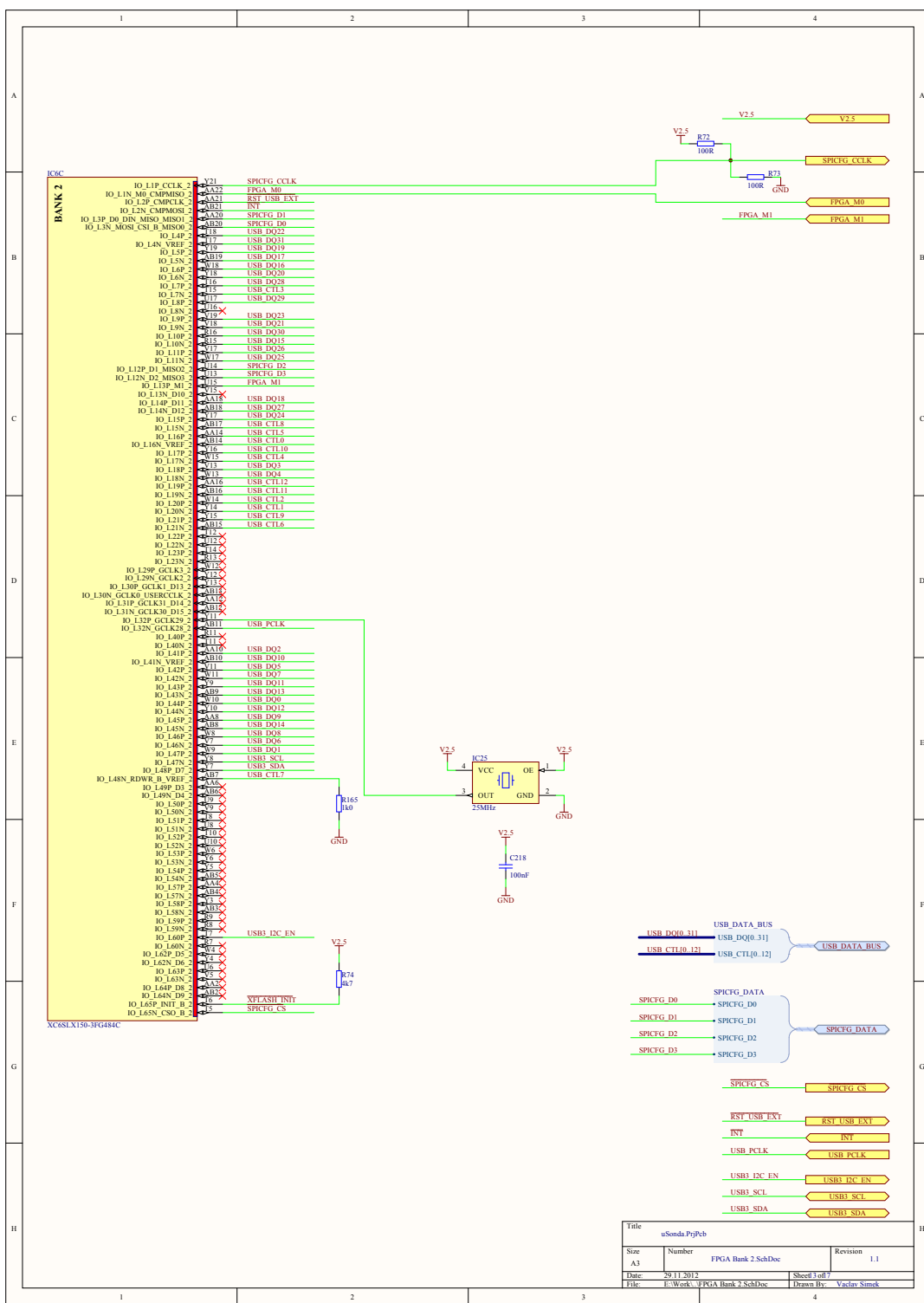


Title			
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Size	A3	Number	FPGA Bank 0.SchDoc
Revision	1.1		
Date	S-11-2012	Sheet left	
File	F:\Work\1\FPGA Bank 0.SchDoc	Drawn By:	Vaclav Smek

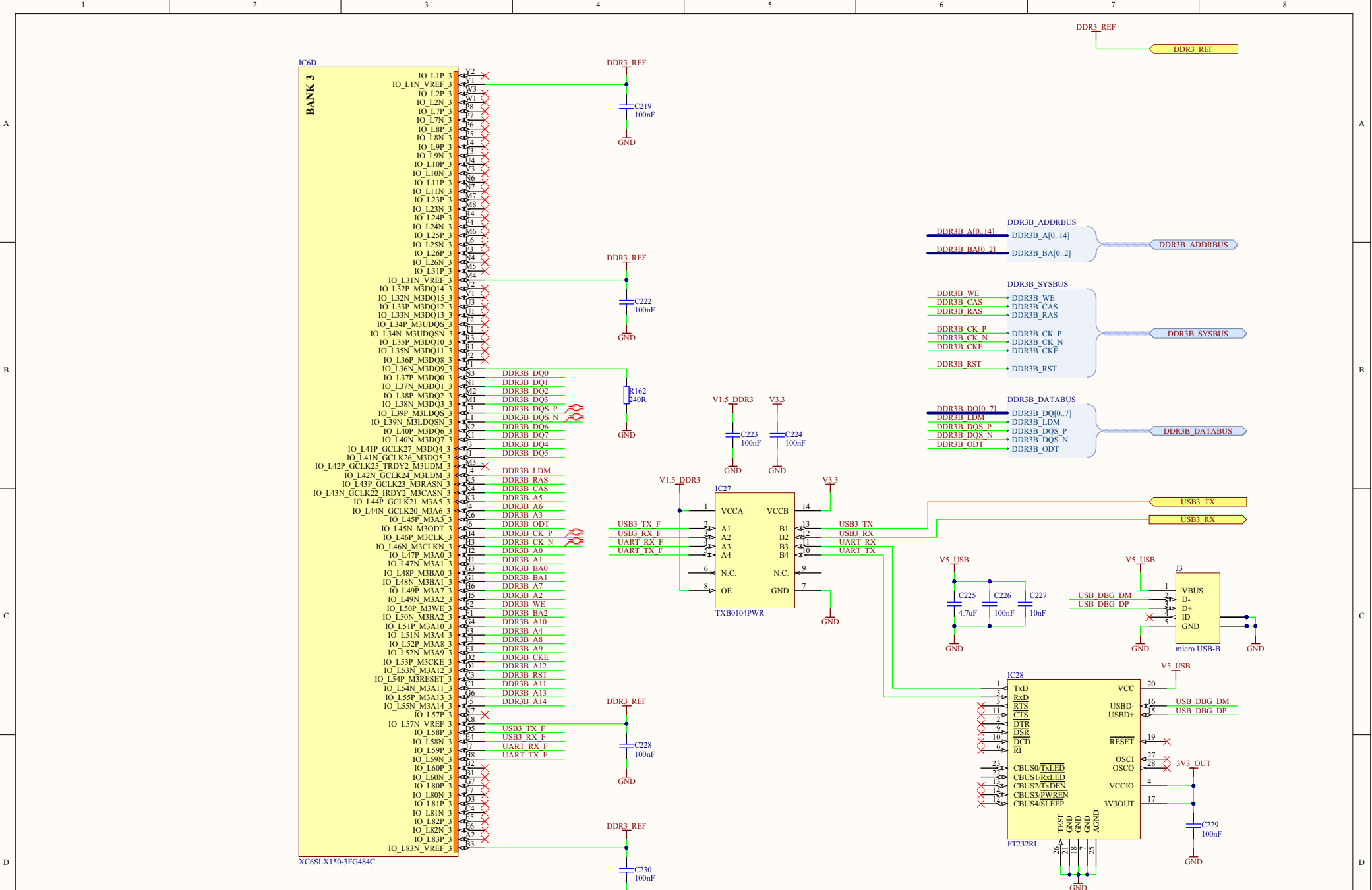


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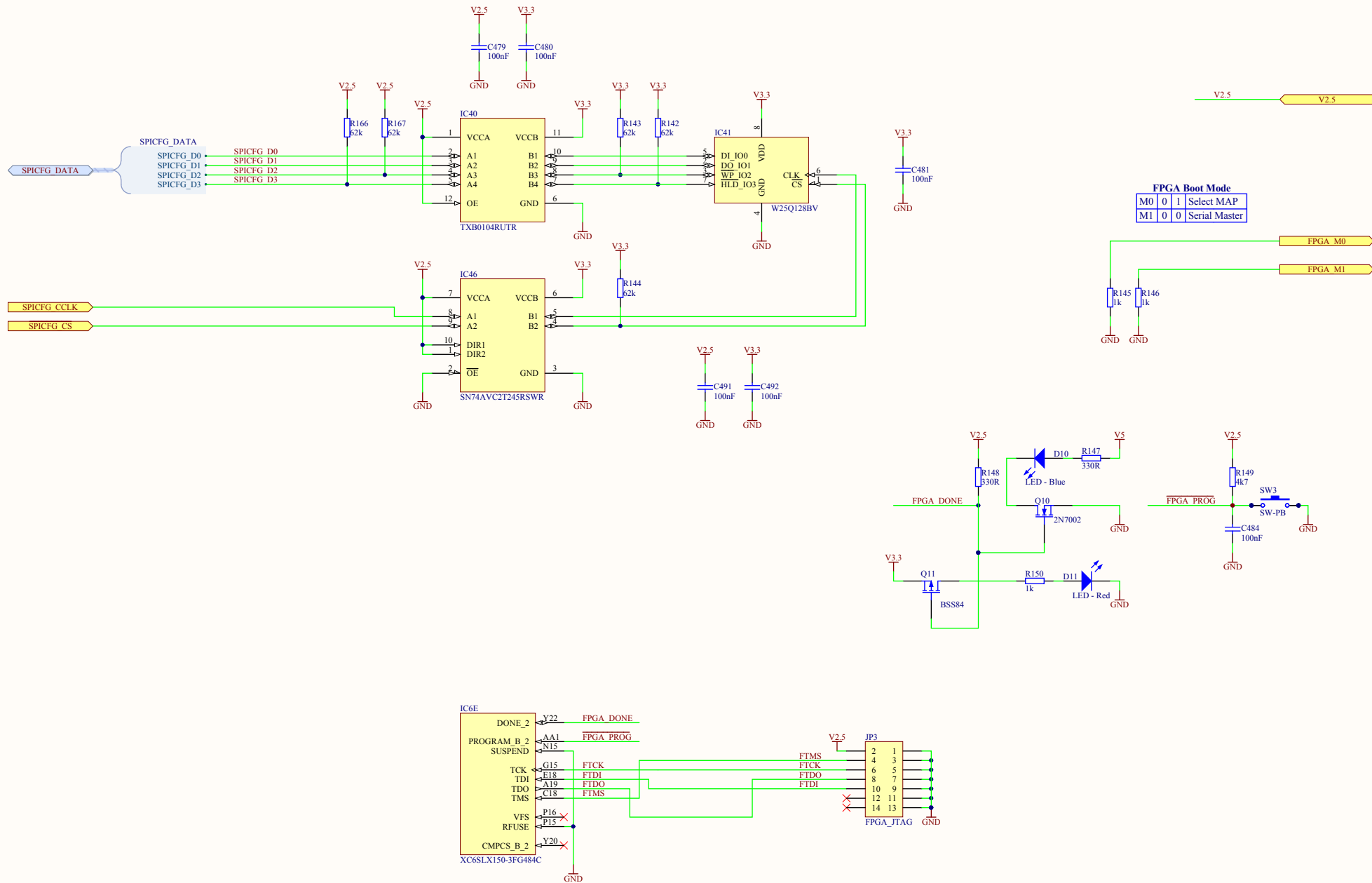
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Size	Number	Revision
A3	FPGA Bank 1.SchDoc	1.1
Date:	29.11.2012	Sheet 2 of 7
File:	E:\Work\...FPGA Bank 1.SchDoc	Drawn By: Vaclav Simek



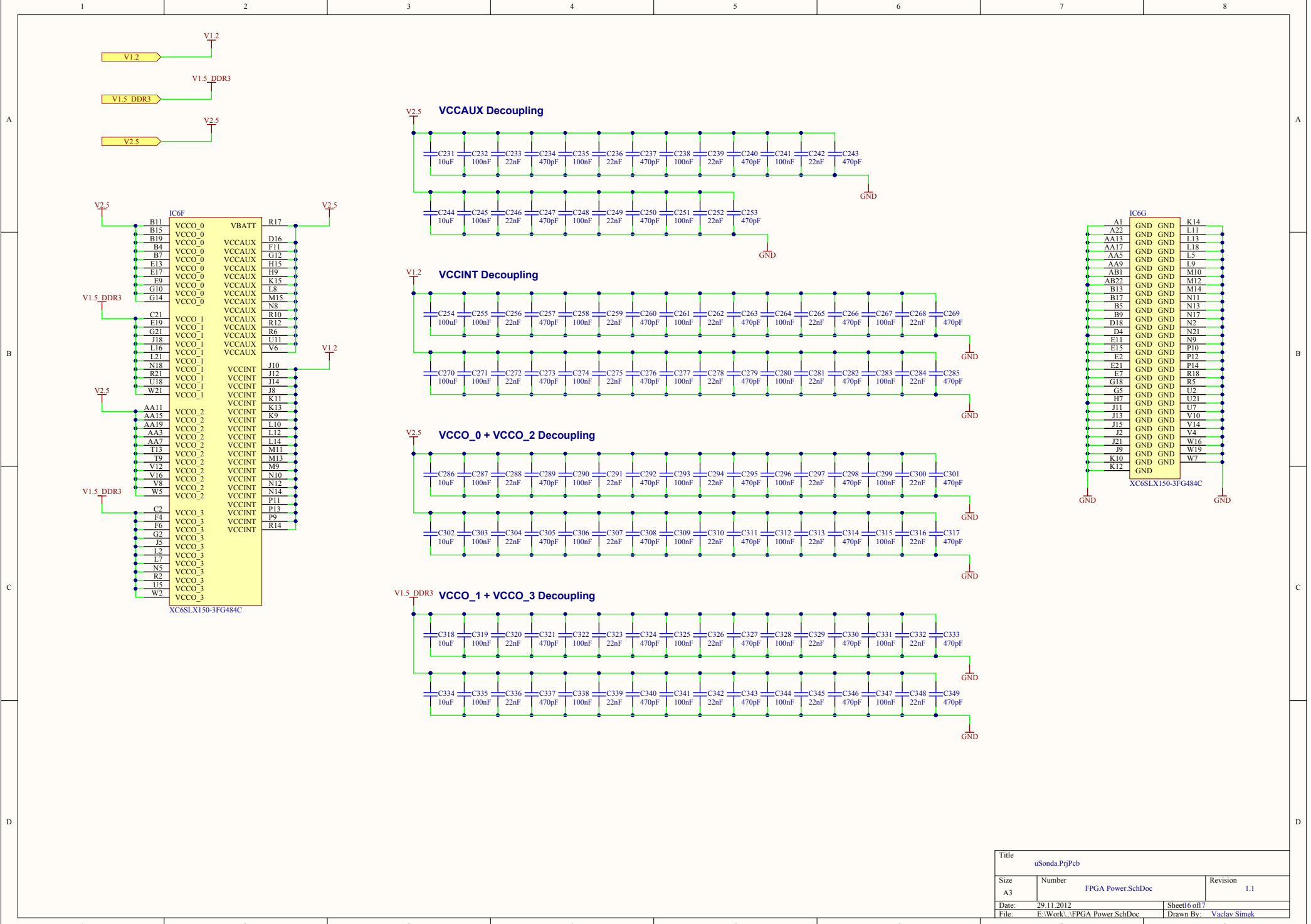
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Size	Number	Revision	
A3	FGA Bank 2.SchDoc	1.1	
Date:	Sheet 1 of 1		
File:	E:\Work\FGA Bank 2.SchDoc	Drawn By:	Vladav Smak



Title			uSonda PrjPcb		
Size	A3	Number	FPGA Bank 3.SchDoc	Revision	1.1
Date:	29.11.2012		Sheet 4 of 7		
File:	E:\Work\...FPGA Bank 3.SchDoc		Drawn By:		Vaclav Simek

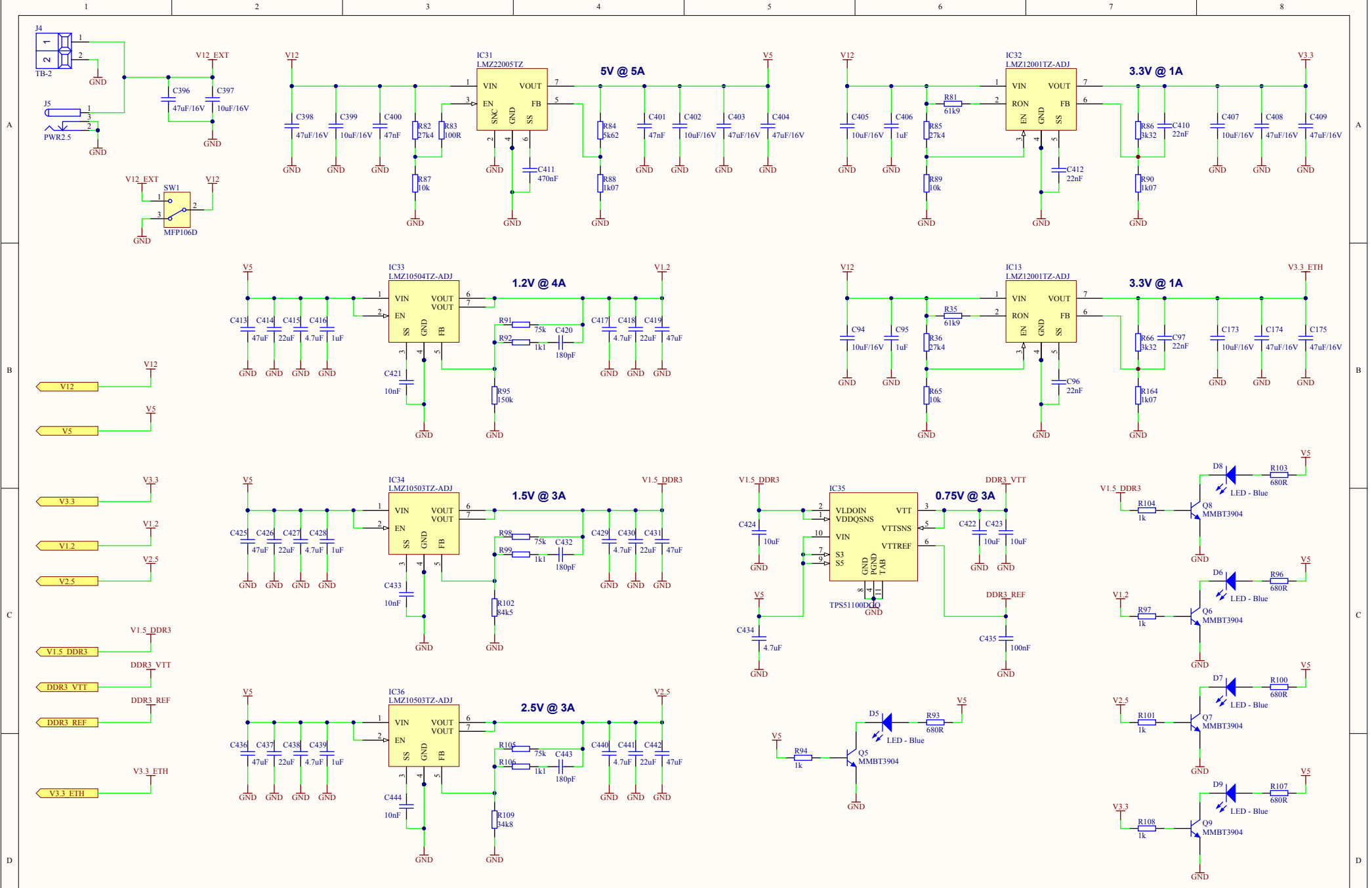


Title			uSonda.PrjPcb		
Size	Number	Revision			
A3	FPGA Config.SchDoc	1.1			
Date:	29.11.2012	Sheet 5 of 7			
File:	E:\Work\...FPGA Config.SchDoc	Drawn By:		Vaclav Simek	



Title			
uSonda.PrjPcb			
Size	Number	Revision	
A3	FPGA Power.SchDoc	1.1	
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File:	E:\Work\...FPGA Power.SchDoc	Drawn By:	Vaclav Simek





Title			uSonda.PrjPcb
Size	Number	Revision	
A3	Board Power.SchDoc	1.3	
Date:	29.11.2012	Sheet17of17	
File:	E:\Work\...Board Power.SchDoc	Drawn By: Vaclav Simek	