

On Complexity of Offline Partial Dynamic Reconfiguration Scheduling

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- topic of my Ph.D. thesis: [The Use of Reconfigurable Architectures in Computer Networks](#)

Partial Dynamic Reconfiguration (PDR)

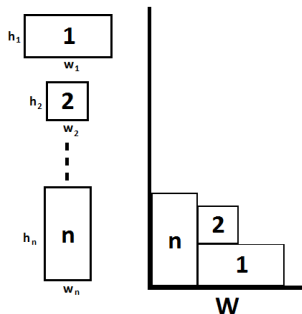
Process of changing configuration of some part of FPGA, while the rest of FPGA is untouched and still working.

- tasks can be time-multiplexed in order to share the same resources
 - we must schedule utilization of resources by tasks
- scheduling of tasks can be studied in terms of the **strip packing problem**



Definition [Lodi et al.]

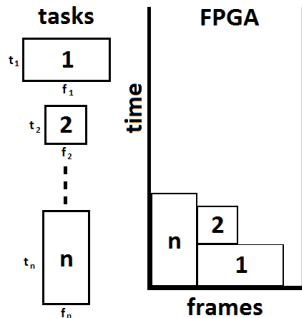
- a set of n rectangular items, each having *width* w_i and *height* h_i , where $i \in 1, \dots, n$
 - a single container (called *strip*) having *width* W and unlimited *height*
 - the task is to pack all items into the strip in such a way that they do not overlap and the height of used strip is minimal
-
- each item has fixed orientation (i.e. items cannot be rotated)
 - we consider an offline version (all parameters are known at the time of packing)
 - the 2SP is **NP-hard** problem (often stated in the literature without proof)





Frame

- the smallest addressable part of FPGA configuration memory
 - 1b column over the full height of FPGA
 - frame's properties reduce the problem dimension by one (2-D instead of 3-D strip packing problem)
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- each **item** models one task
 - *width* – the number of used frames
 - *height* – processing time of the task
 - **strip** models available resources
 - *width* – the number of frames within FPGA
 - *height* – run time of the whole system



Decision Problem [Češka 2009]

- a decision problem P can be understood as a function f_P with the range $\{true, false\}$
- a decision problem is usually specified by
 - the set I_P of possible instances of the problem P
 - the subset $A_P \subseteq I_P$, $A_P = \{p \in I_P \mid f_P(p) = true\}$ of instances for which f_P evaluates to *true*

Optimization Problem [Černá 1998]

- an optimization problem P is specified by
 - the set I_P of possible instances of the problem P
 - the function F assigning each instance $x \in I_P$ a set of feasible solutions
 - the function v assigning each $r \in F(x)$ its value $v(r) \in \mathbb{Q}^+$
- we look for feasible solution with either **maximal** or **minimal** value
- each optimization problem has an associated decision problem

h-bin packing problem [Černá 1998]

- the h-bin packing problem is specified by
 - a set of n items, each having *weight* w_i , where $i \in 1, \dots, n$
 - a set of k bins, each having *weight limit* W
- the question is whether it is possible to divide all items between bins in such a way, that no weight limit is violated
- h-bin packing problem is **NP-complete**

1-dimensional bin packing problem (1BP) [Lodi et al.]

- the 1BP is specified by
 - a set of n items, each having *weight* w_i , where $i \in 1, \dots, n$
 - an infinite number of bins, each having *weight limit* W
- the task is to divide items into bins in such a way, that no weight limit is violated and the number of used bins is minimal
- the h-bin packing problem is a decision problem associated with the 1-dimensional bin packing problem



Lemma 1

- an optimization problem is NP-hard iff its associated decision problem is NP-complete
- for details see [Černá 1998], page 85

Proof of 2SP NP-hardness

- the h-bin packing problem is NP-complete and it is a decision problem associated with 1BP
- from previous and Lemma 1 we get NP-hardness of 1BP
- 1BP is a special case of 2SP
 - width of items are represented by their weights
 - height of items are set to $h_i = 1$, where $i \in 1, \dots, n$
 - width of the strip is represented by weight limit of bins
- if 1BP (special case) is NP-hard, then 2BP (general case) must also be NP-hard





Organization of configuration memory in modern FPGAs

- the smallest addressable area is still frame, but it does not span the whole FPGA height anymore
- we should consider the 3-dimensional strip packing problem

Heterogenous FPGA structure

- except logic blocks, there are blocks of on-chip memory, multipliers, etc.
- heterogenous FPGA structure imposes additional restrictions on tasks' scheduling

Communicating and timing issues

- tasks must be placed at such positions in FPGA's structure, that they meet timing constraints and are able to communicate with the rest of the system
- in terms of formal model, this means introducing further restrictions



- scheduling the reconfiguration of tasks implemented on FPGAs can be studied in terms of the 2-dimensional strip packing problem
 - we have studied an offline version of 2SP, but sometimes an online version could be the case
- it has been proven that 2-dimensional strip packing problem is NP-hard
 - within the proof we have used the h-bin packing problem and the 1BP
- limitations of presented formal model regarding to modern FPGAs have been discussed
 - it would be necessary to use 3-dimensional strip packing problem and impose far more restrictions on the model



- [Lodi et al.] A. Lodi, S. Martello and D. Vigo: [Models and Bounds for Two-Dimensional Level Packing Problems](#), *Journal of Combinatorial Optimization*, Vol. 8, pp. 363-379
- [Češka 2009] M. Češka and T. Vojnar: [Theoretical Computer Science TCS: Textbook](#), FIT BUT, January 2009
- [Černá 1998] I. Černá: [Úvod do teórie zložitosti](#), FI MU, February 1998