Fault tolerant system — design of reconfigurable controller methodology

Richard Pánek
xpanek06@stud.fit.vutbr.cz

October 13, 2016

Not only rate and complexity demands but also reliability demands on fault tolerant systems implemented by digital circuits are permanently increasing. The fulfilment of the reliability requirements is the goal of the techniques denoted to as the design of fault tolerant systems. The goal of this techniques are to prevent faults or be able to recover from them. Nowadays, the fault tolerant systems are often implemented into FPGA (Field Programmable Gate Arrays). Thanks to its reconfiguration capabilities, we are able to change the configuration of the FPGA and thus reestablish its correct functionality when any faults are detected.

The dynamic reconfiguration controller is an important component of fault tolerant systems. It must be able to modify the circuit and thus repair any faults that have been identified. The dynamic reconfiguration means that when any faults are detected the circuit is reset to its correct state during its operation. Several approaches exist for the controller construction. The controller can be implemented either directly in FPGA together with the desired circuit or out of the reconfigurable element. In first case, a useful technology is a partial dynamic reconfiguration. However, this controller occupies same sources of FPGA which cannot be then used to implement the required function. In addition, it is necessary to take into account the requirement on the power consumption of the controller. The second possibility is a full dynamic reconfiguration controlled by the element which is located out of the part of the system which is reconfigured. The main advantage of this solution is the possibility to use all the resources of the FPGA. On the other hand, with the increasing information content about the function of the circuit (bitstream) the required reconfiguration times are increased too. Furthermore, there are two possibilities for the implementation the external controller, the first case is by using the electronic element. The second possibility lies in the program for microprocessor or microcontroller.

Another aspect increasing the overall complexity of the circuit can be the requirement to construct the reconfiguration controller as fault tolerant itself. This requirement will have the impact on the time needed to complete the reconfiguration and thus on the performance of the element. Another important aspect is the size of the components that are to be reconfigured. Based on to requirements on the fault tolerant system the controller is either able to reconfigure periodically which allows us to achieve fault prevention or it reconfigures the circuit only when some fault is detected which just provides fault recovery capabilities.

The goal of this research is to apply formal approaches in the dynamic reconfigurable controller design which will reflect the above mentioned alternatives.