IMPROVING REGISTER USAGE

Compiler construction 2013/2014

abstract

… talk will be given by Michal Samek and Martin Foukal

Increasingly, the performance of a modern computer system is determined by the performance of its memory hierarchy. While on-chip operation speeds have been dramatically improving, the performance of memory has mostly remained constant. As a result, the latencies to main memory in terms of processor cycles have been increasing. These latencies must be ameliorated if the machine performance is to keep pace with the performance of the processor. [1]

During the talk, there will be introduced common compiler transformations for improving register usage, such as *scalar register allocation, unroll-and-jam* and *loop interchange*. We will try to focus mainly on the basic principles and limitations (legality) of these method. Afterwards we will present *loop interchange* or *scalar register allocation* in a greater depth.

[1] Improving Register Usage. ALLEN, Randy a Ken KENNEDY. *Optimizing compilers for modern architectures: a dependence-based approach*. San Francisco: Morgan Kaufmann, c2002. ISBN 978-1-55860-286-1.