SAT-based equivalence checking of polymorphic circuits

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Abstract

Polymorphic (or multifunctional) digital circuits represent a special category of integrated circuits with the ability to perform two or more logic functions according to given input control signals. The logic function can be selected with the aid control signals, which may include power supply voltage level or ambient temperature of a polymorphic circuit. These circuits are made up of several polymorphic gates, that are mostly designed with CMOS technology.

In computer science, a satisfiability (often known as SAT) is a subject of matter related to the question, whether there is a specified expression (formula) denoted in boolean logic operations using only AND, OR, and NOT assignment, in which the expression evaluates to true. It is also important to determine if the expression of any such assignment exists. In fact, such observation would imply that the specified function in terms of a set of formulas is contradiction (ie, that when any input is the output value FALSE) - under such circumstances we claim the function is unsatisfiable, otherwise just the opposite is valid.

Conventional approach for synthesis of polymorphic circuits does not achieve an efficient solution. So there has been obvious effort to develop highly refined methods for the last couple of years. However, these methods are applicable only for circuits with a small number of gates.

This work is dealing with a deployment of SAT problem in order to streamline the synthesis of polymorphic circuits. The most time-critical section of CGP circuit design can be attributed to the corectness evaluation of a proposed circuit. The proposed algorithm, as discussed in [1], aims to reduce the period of time dedicated to circuit evaluation through the direct exploitation of SAT for equivalence checking and also optimize the resulting polymorphic circuit as well.

References

[1] Lukas Sekanina and Zdenek Vasicek. A SAT-based fitness function for evolutionary optimization of polymorphic circuits. *Proc. of the 2012 Design, Automation and Test in Europe*, 1:715–720, 2012.