COVERAGE DIRECTED CONSTRAINT RANDOM TEST GENERATION AND CONSTRAINT SATISFACTION PROBLEM

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Abstract

In presentation I would like to introduce listeners to the verification technique called coverage directed constraint random test generation (CDTG). It is a technique that extends the simulation based verification (SV) and constraint random test (CRT) generation method. Since we are interested in certain scenarios when we are verifying circuit, using CRT we define constraints that cover these scenarios. Some parts of the verified circuit may remain uncovered or untested and therefore we must manually specify next constraints. CDTG adds principles of automatic control simulation and adds additional constraints using feedback from the result of the coverage analysis. Automatically adjust of verification using feedback aims to control test scenarios to achieve or at least get closer to the 100% coverage of all functions of the circuit. To generate certain scenarios it is necessary to solve the constraints and then by the result modify or generate the additional constraints that achieve the highest coverage.

Hence CDTG methods are equivalent to a constraint satisfaction problem (CSP). Constraint satisfaction problems (CSPs) are mathematical problems that are similar to the problems with we encounter in everyday life. These are defined as a set of objects that must satisfy a number of constraints or limitations. Their possible way of solving is with the constraint solver. Examples of CSPs are N Queens problem and car sequencing problem, which will be discussed in the presentation.

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